Orange County Chapter of the IPC Designers Council, Inc.
presents:

Cause and Effect – How little design issues can cause big headaches to assemblers and fabricators.

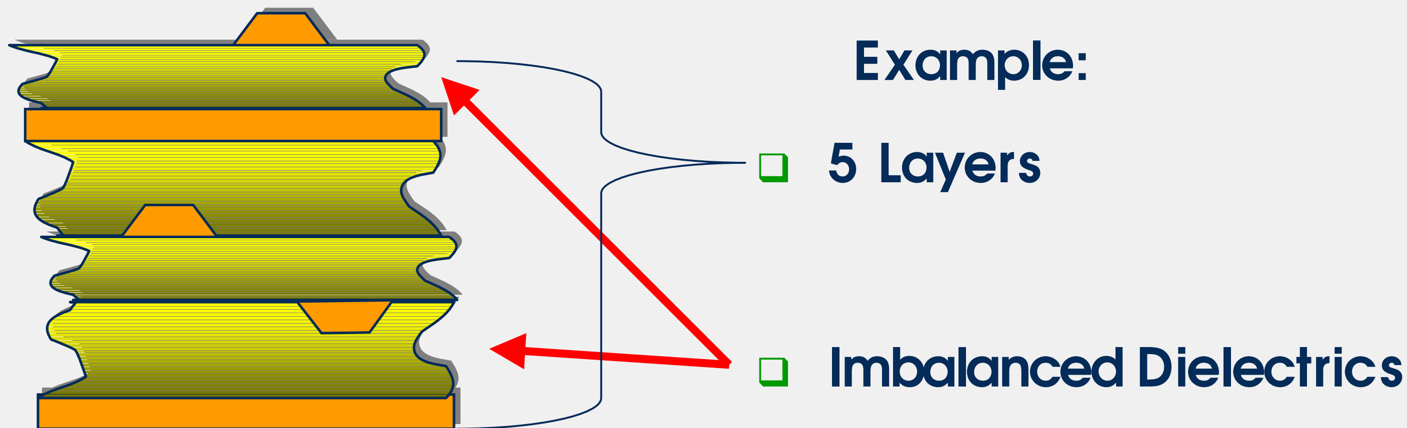
Kathy Palumbo, CEO and Founder -

Dave Kendrick, PCB Designer -

David Hoover, Field Application Eng -

Key Issues for Discussion
(from a fabrication perspective)

- Bow and Twist
  - Unbalanced Stackups – What are the Causes?
    - Odd Number of Layers
    - Nonsymmetrical Dielectrics or Material Types

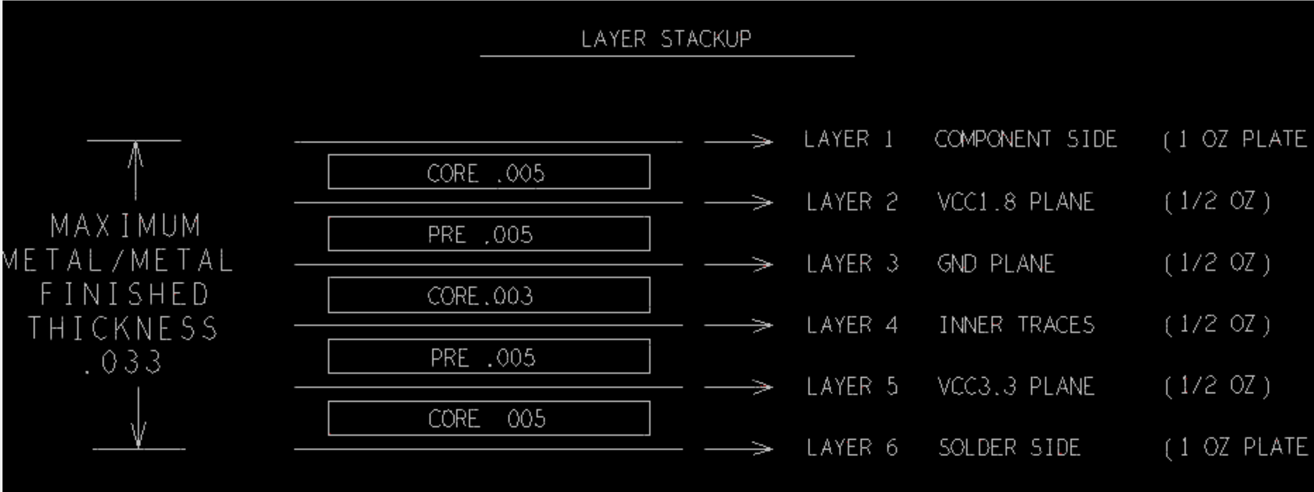


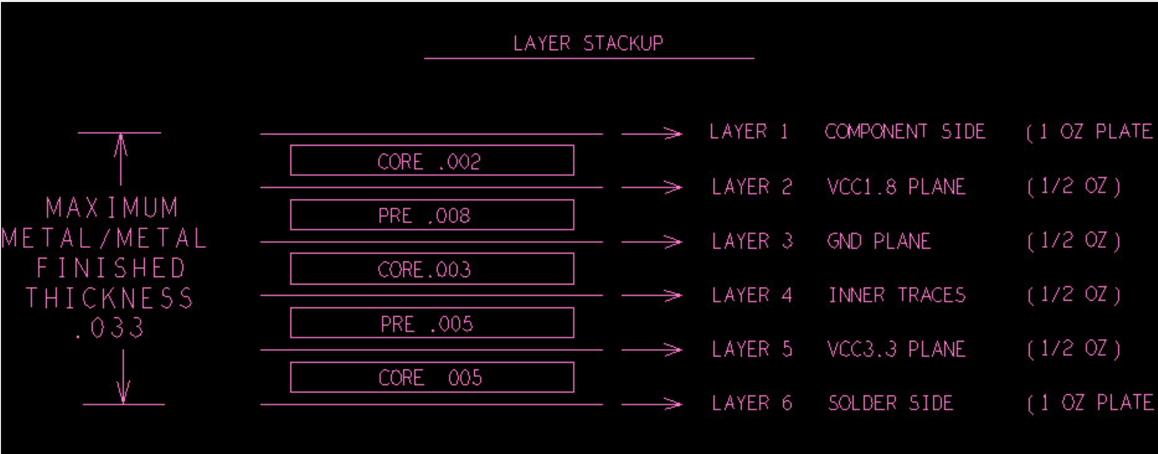
Example:

- 5 Layers
- Imbalanced Dielectrics

Key Issues for Discussion
(from a designer's perspective)

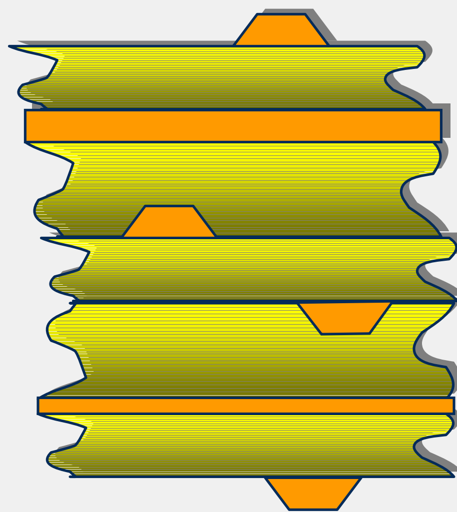
- Bow and Twist
  - Stackups and Print Specifications





Key Issues for Discussion -
(from a fabrication perspective)

- **Bow and Twist**
  - **Unbalanced Stackups – What are the Causes?**
    - **Unbalanced Copper Foil Weights**
    - **Unbalanced Copper Distribution on the Layers (circuitry)**



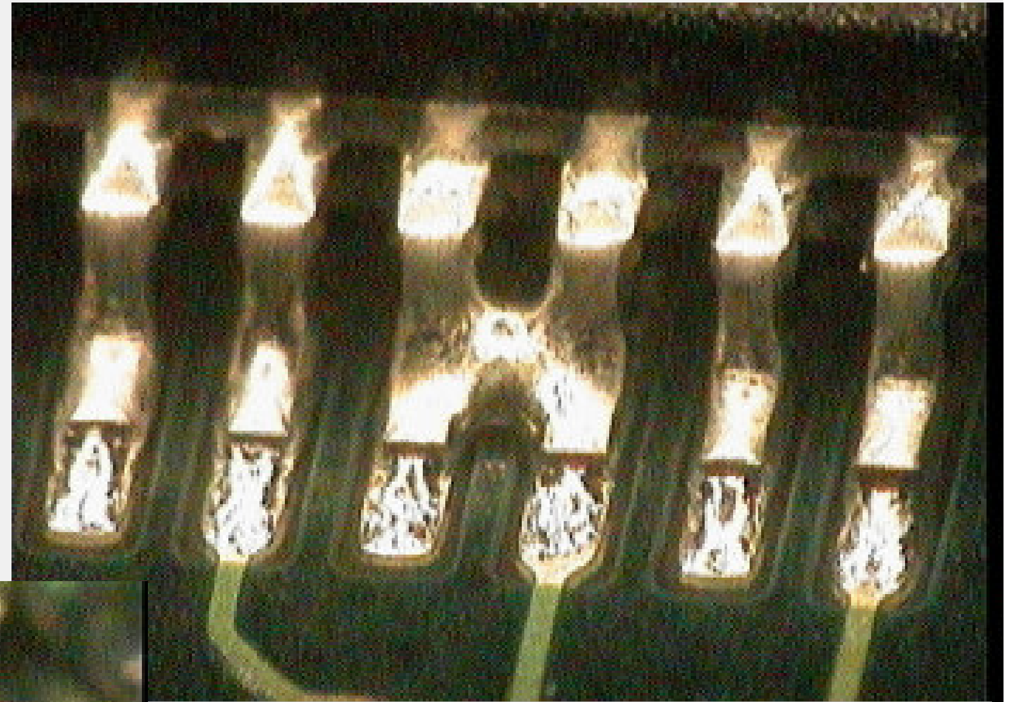
- **Copper Foil Weights**
- **Unbalanced Circuitry**

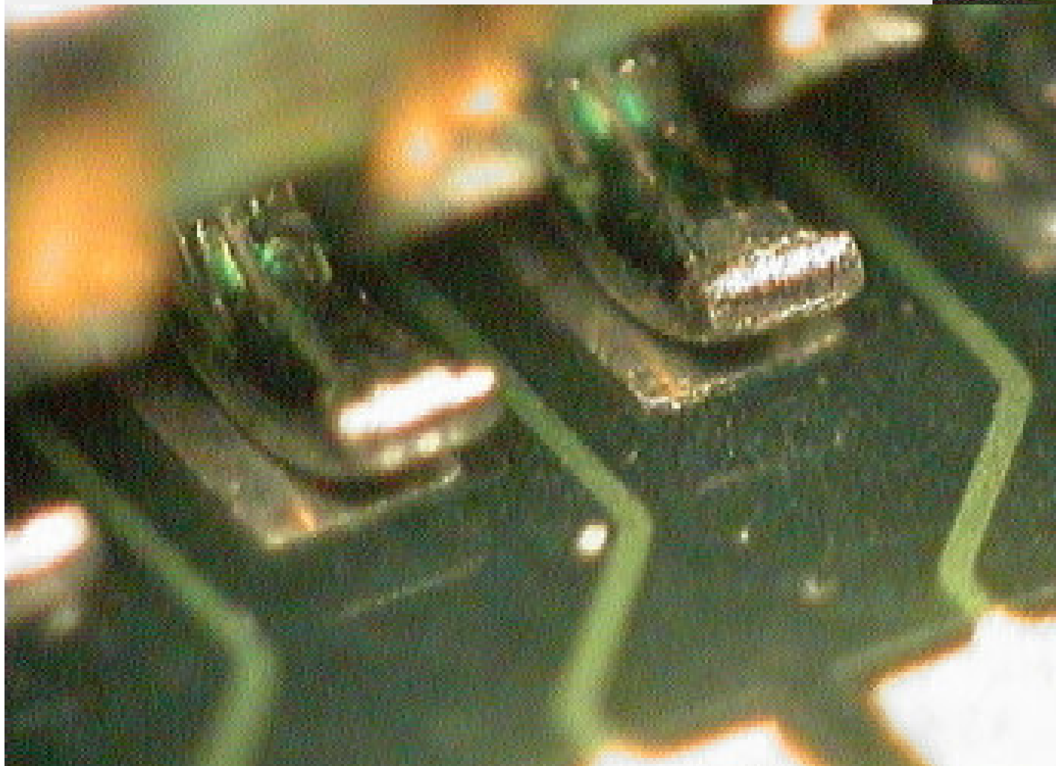
  (e.g., RF and digital designs that have large open laminate areas or large metal shield/planes areas)

Key Issues for Discussion - (from a assembly perspective)

- **Bow and Twist**

Bow and Twist issues are a nightmare at assembly because the screen print process requires a flat planar surface…Remember the Gasket Effect…in order to achieve acceptable paste deposition.

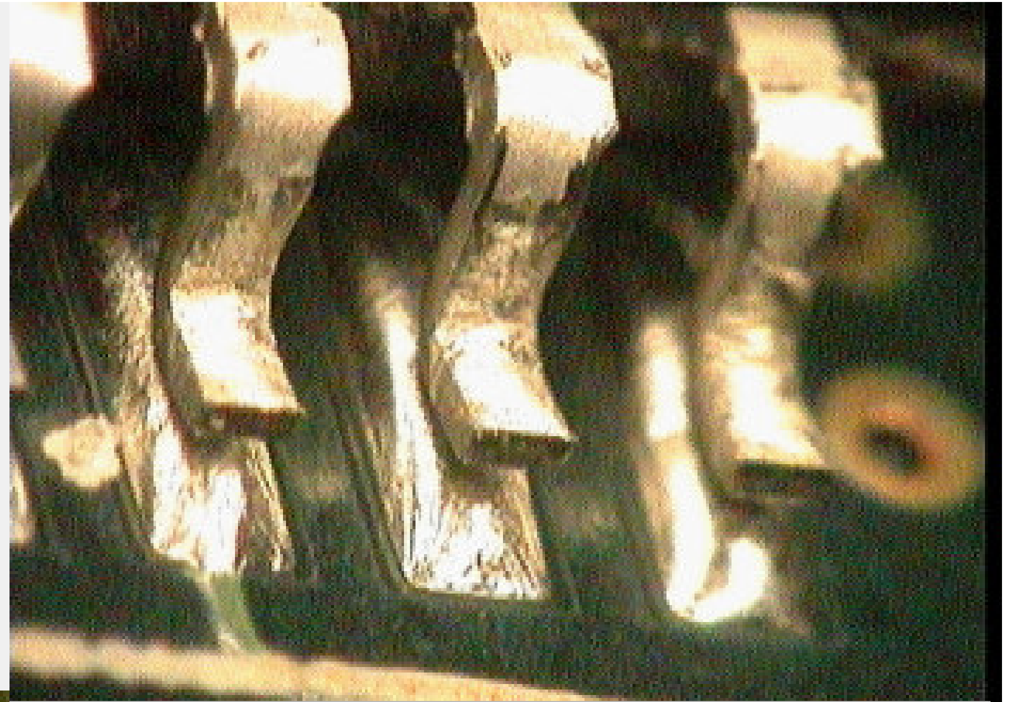


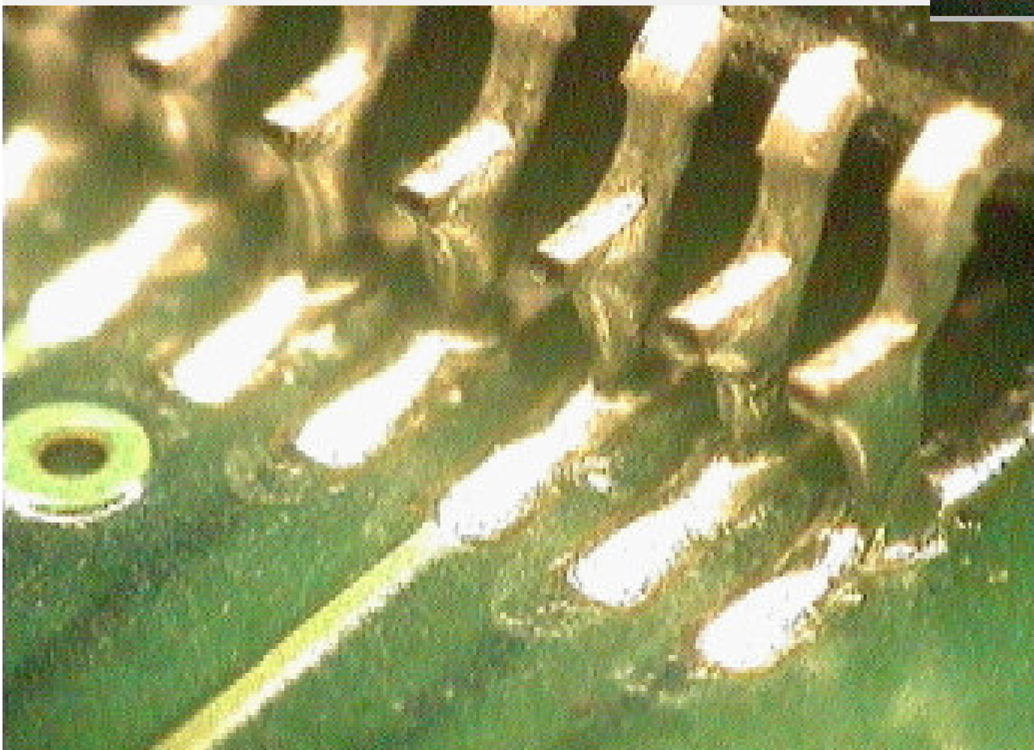


Bow and Twist always leads to misprints which results in bridges and insufficient solder

Surface Mount leads must sit on a planar surface in order for them to solder properly.

Bow and Twist issues can result in opens when surface mount leads can not sit planar.

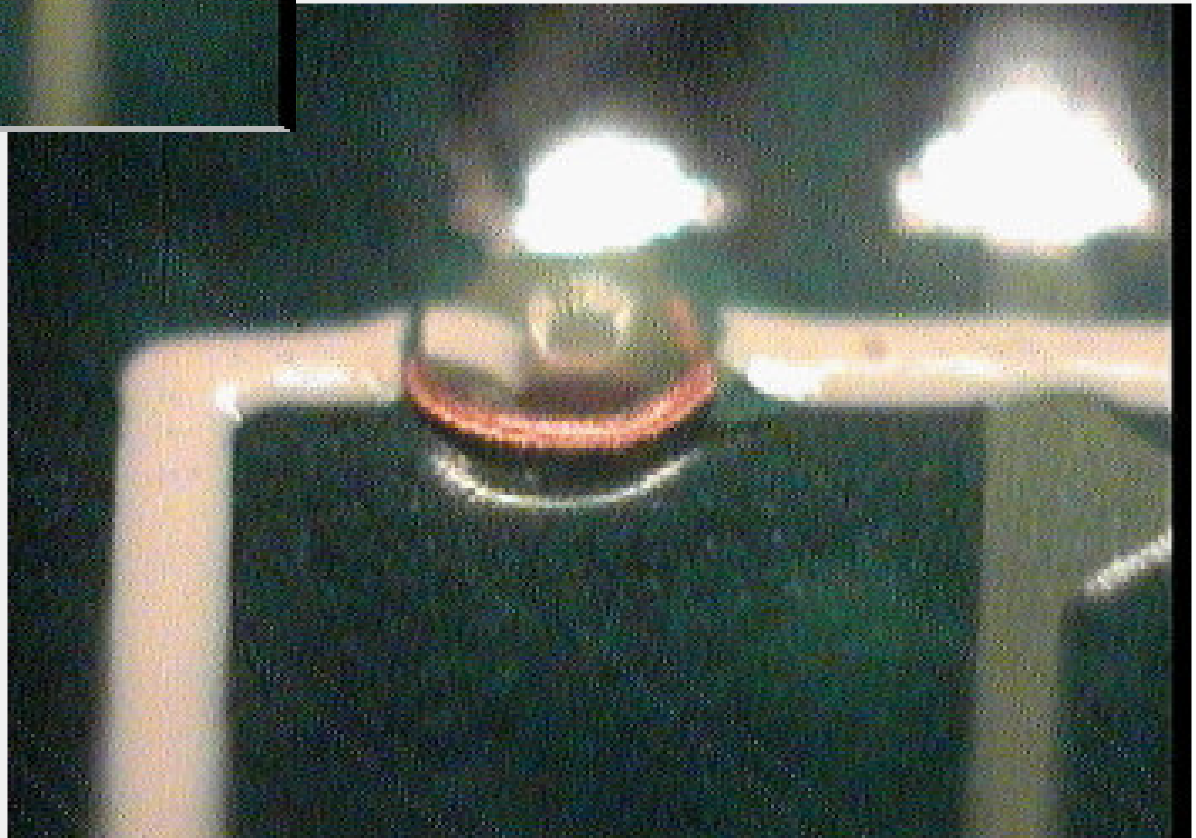




PCB's with Bow and Twist issues can not be made to sit planar. A PCB with a bow and twist issue is in its natural state.

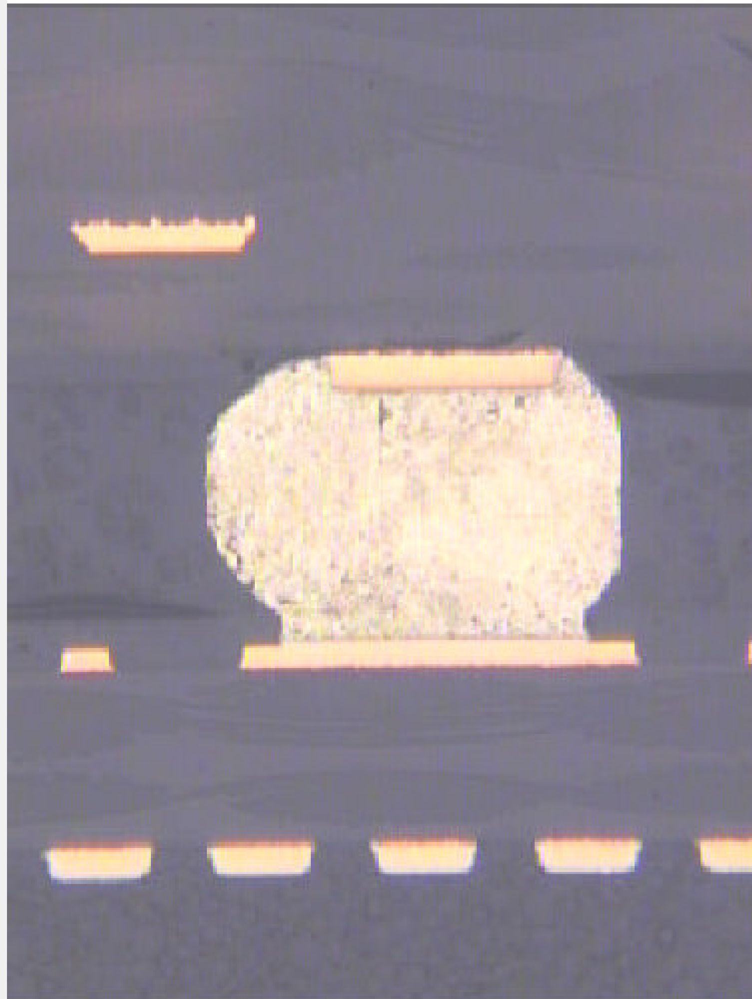
When a PCB is forced to lay flat by baking, and then thermally cycled in a reflow process it will always go back to its natural bow and twisted state. This always results in lifted leads.

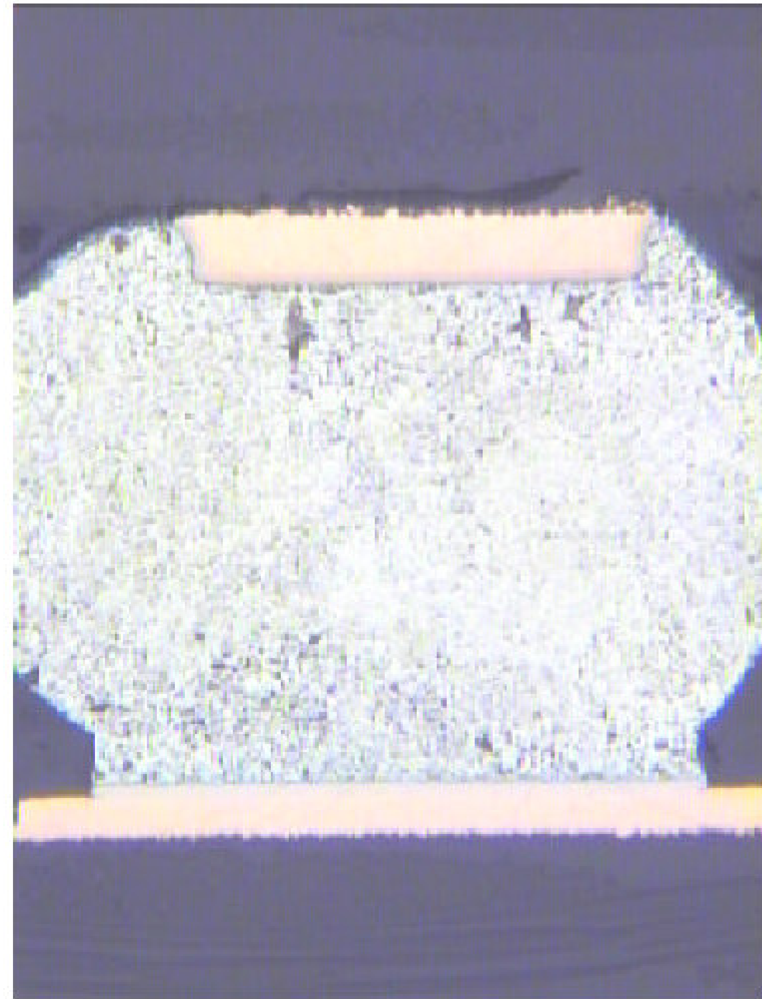
A PCB with a Bow and Twist issue that is forced to lay flat can result in other issues during the SMT convection oven process.



This PCB had a Bow and Twist issue that was forced to lay planar, and when reflowed in a SMT convection oven process the Via's exploded causing components to fly off the PCB.

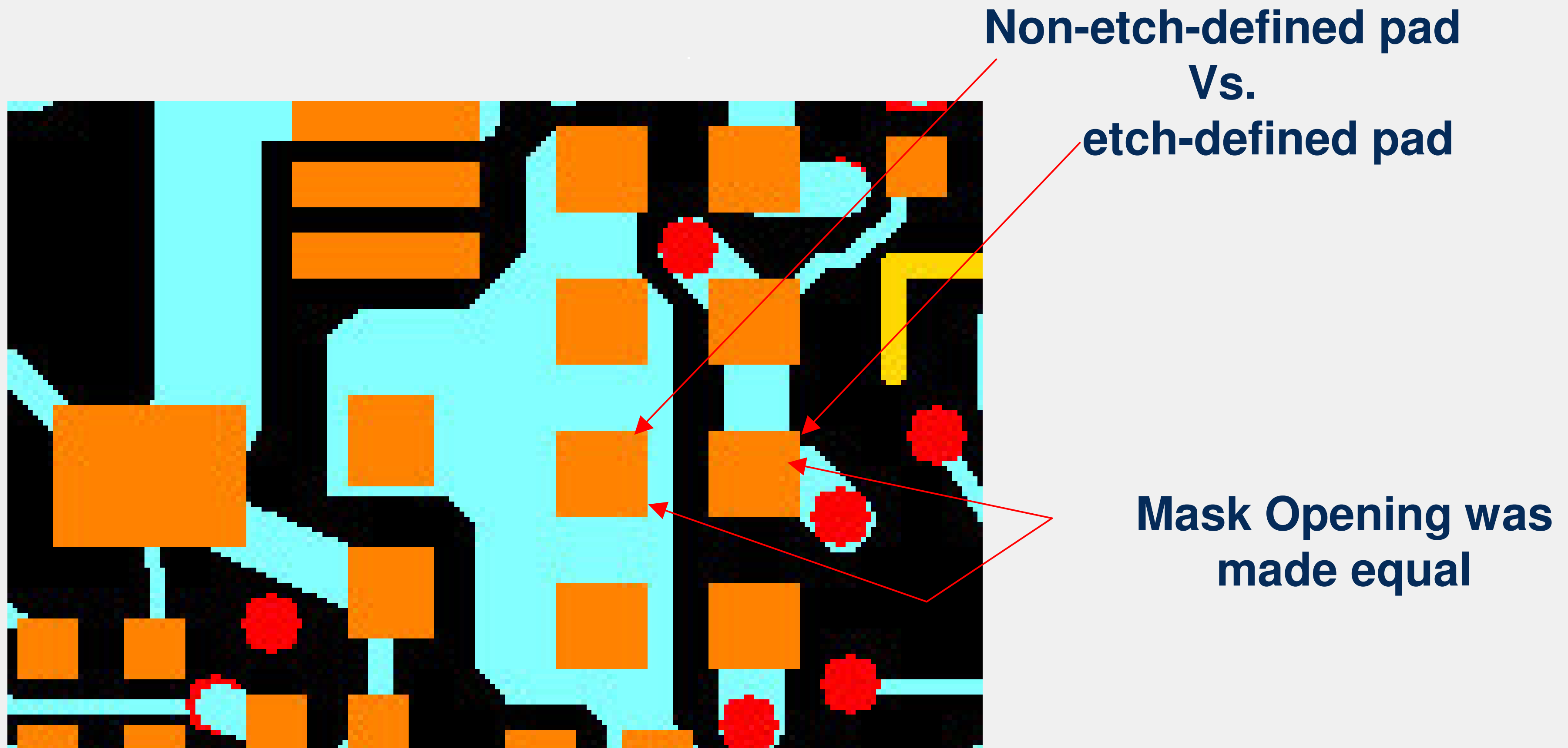
This PCB had a Bow and Twist issue and was forced to lay planar, which resulted in Laminate tears during thermal cycling of the completed assembly.





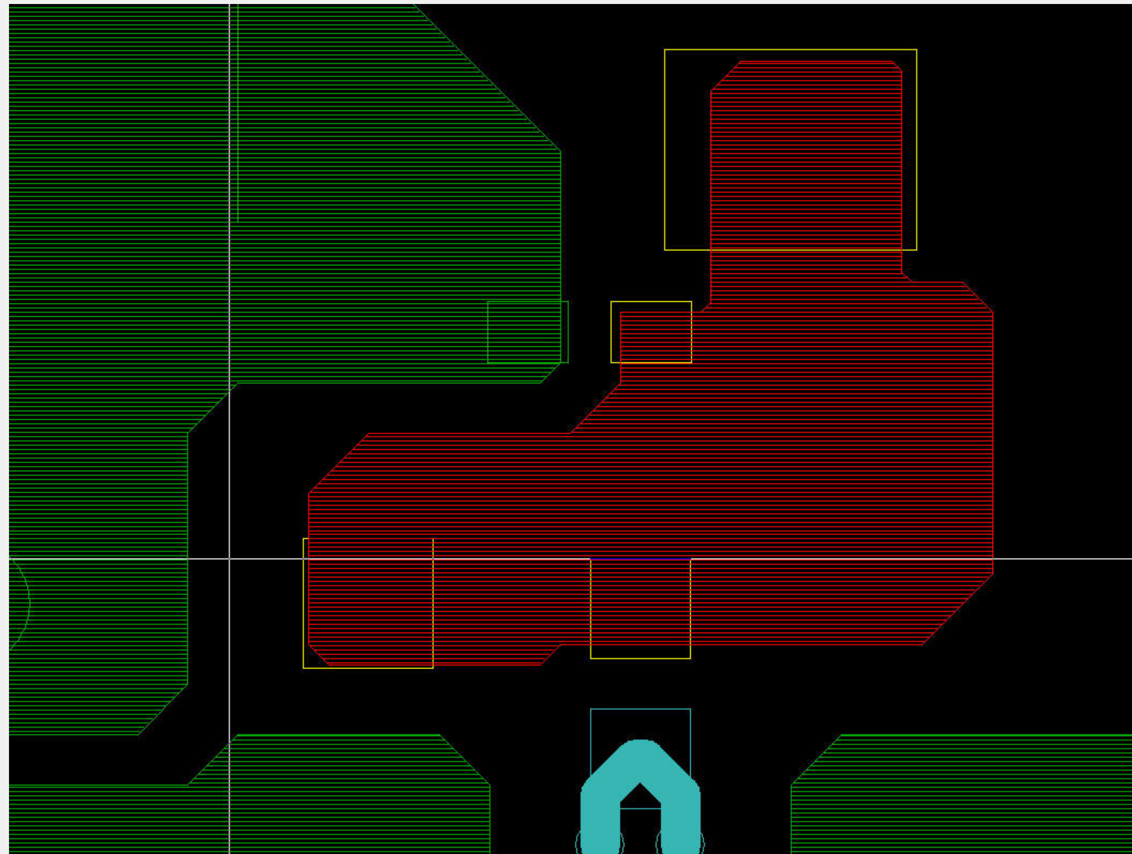
Key Issues for Discussion - (from a assembly perspective)

- **Non-Symmetrical Pads** (nightmares at assembly; etch-defined pads; how to avoid issues at the design level)



Key Issues for Discussion - (from a designer's perspective)

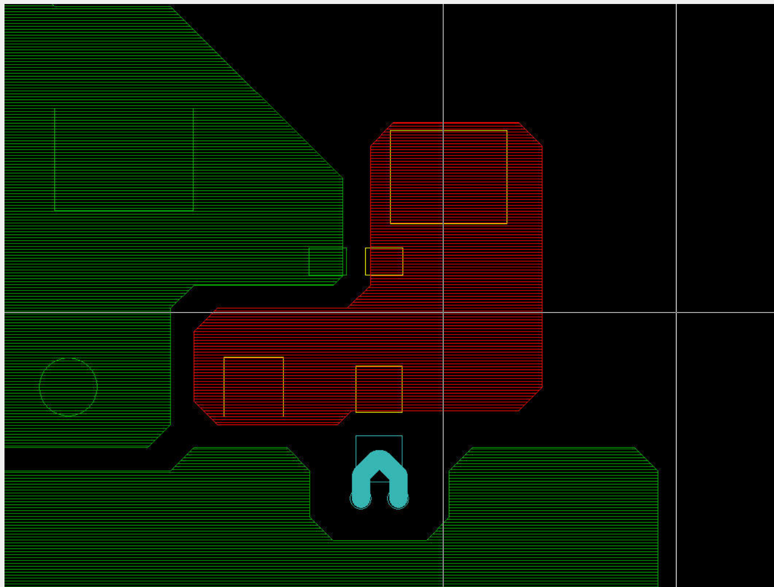
- **Non-Symmetrical Pads** (etch-defined pads)



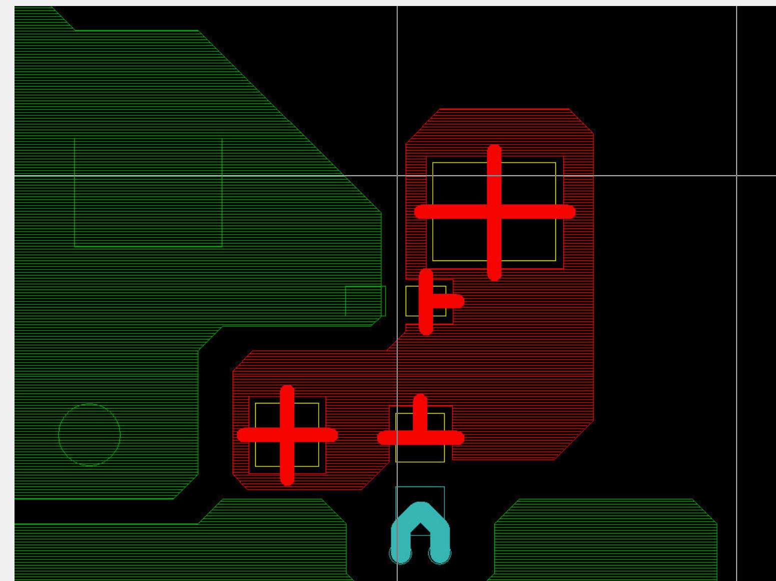
Exposed Edge Defined

Key Issues for Discussion - (from a designer's perspective)

- **Non-Symmetrical Pads** (etch-defined pads)

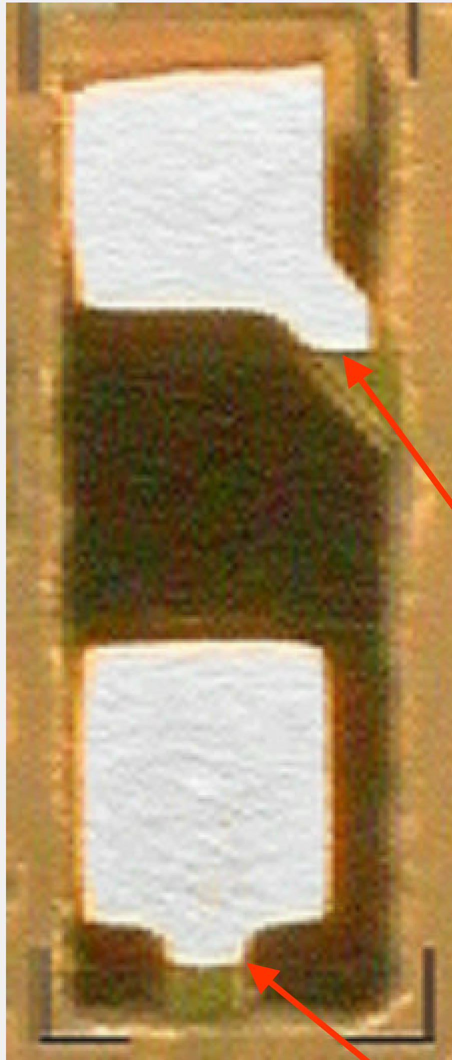


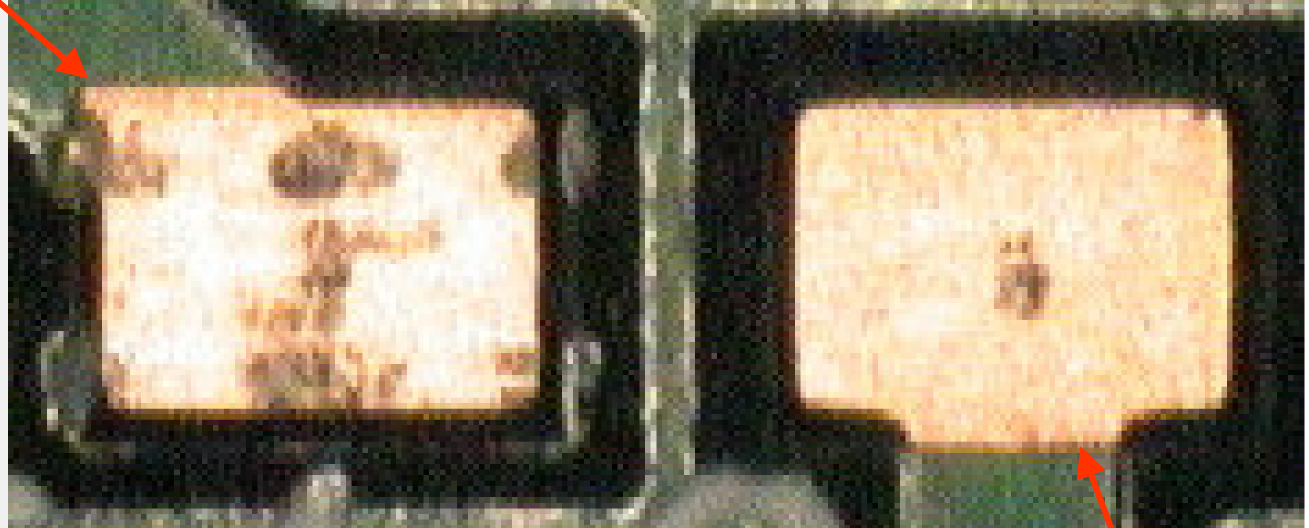
Non-Thermal Defined

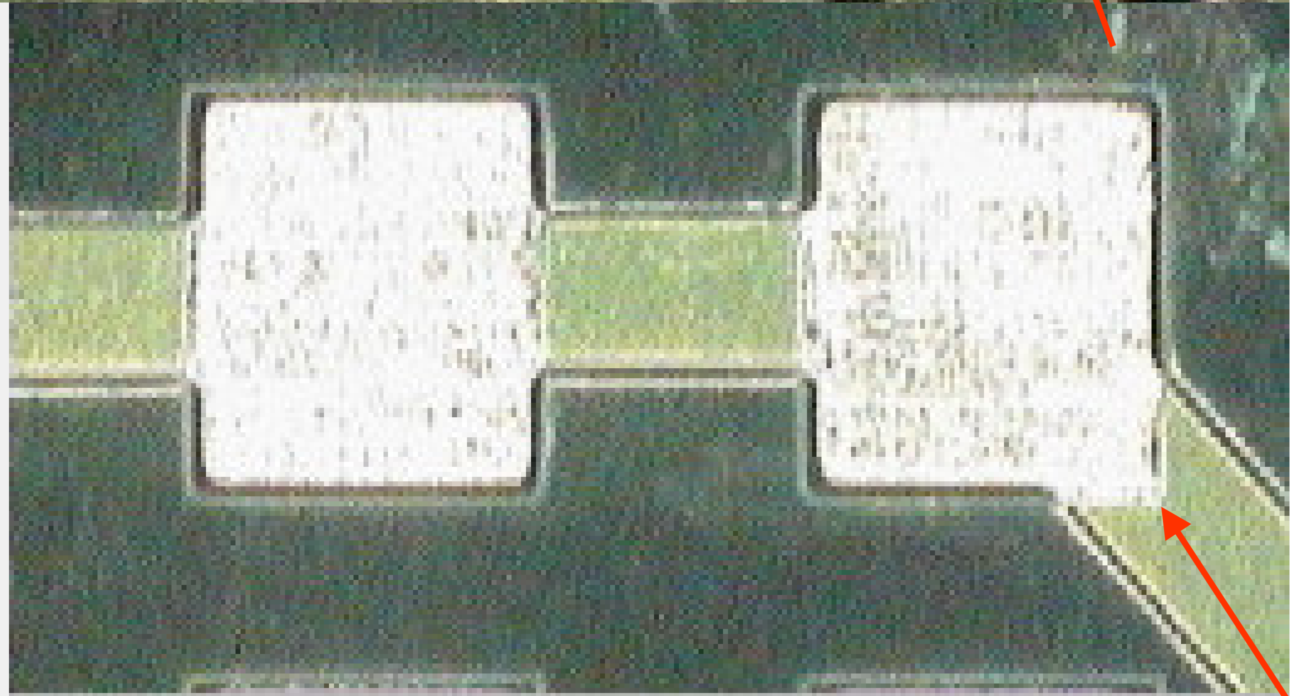


Thermal Defined

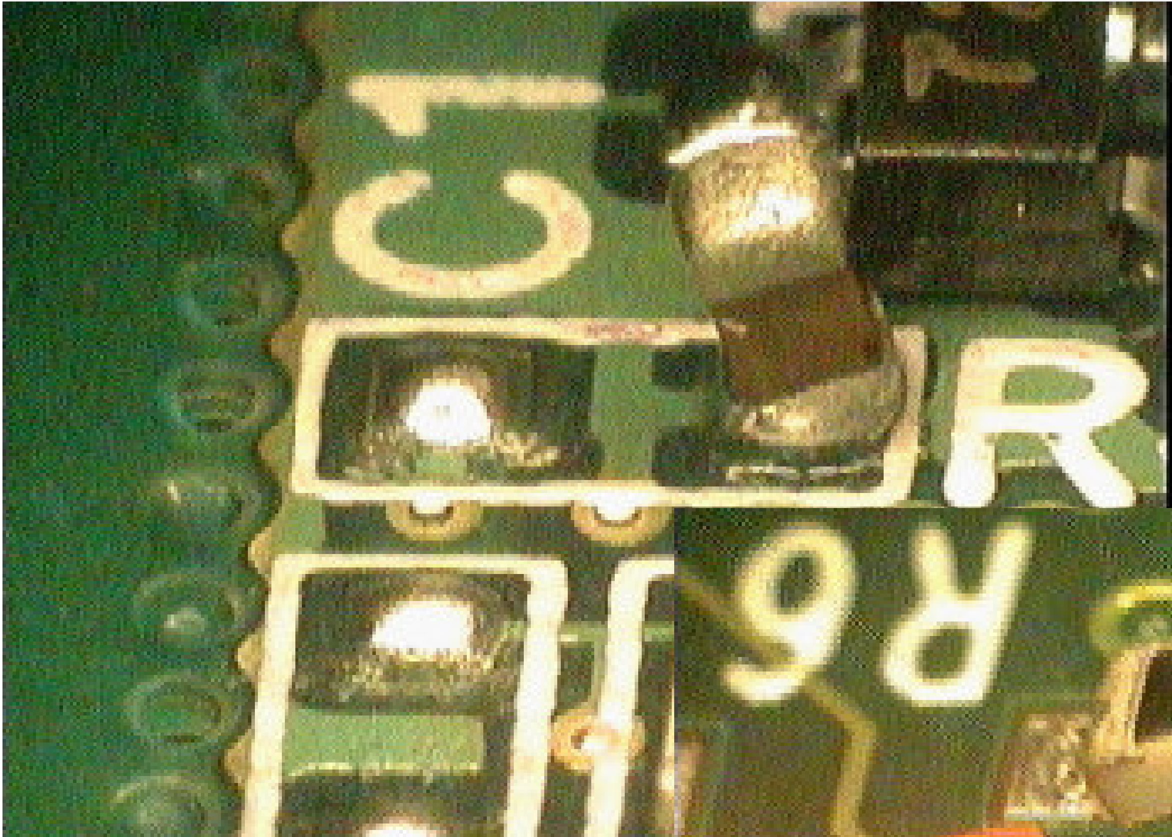
Mask Openings that are made Equal for a non-etched defined pad Vs a etched defined pad will always result in Non-Symmetrical Pads

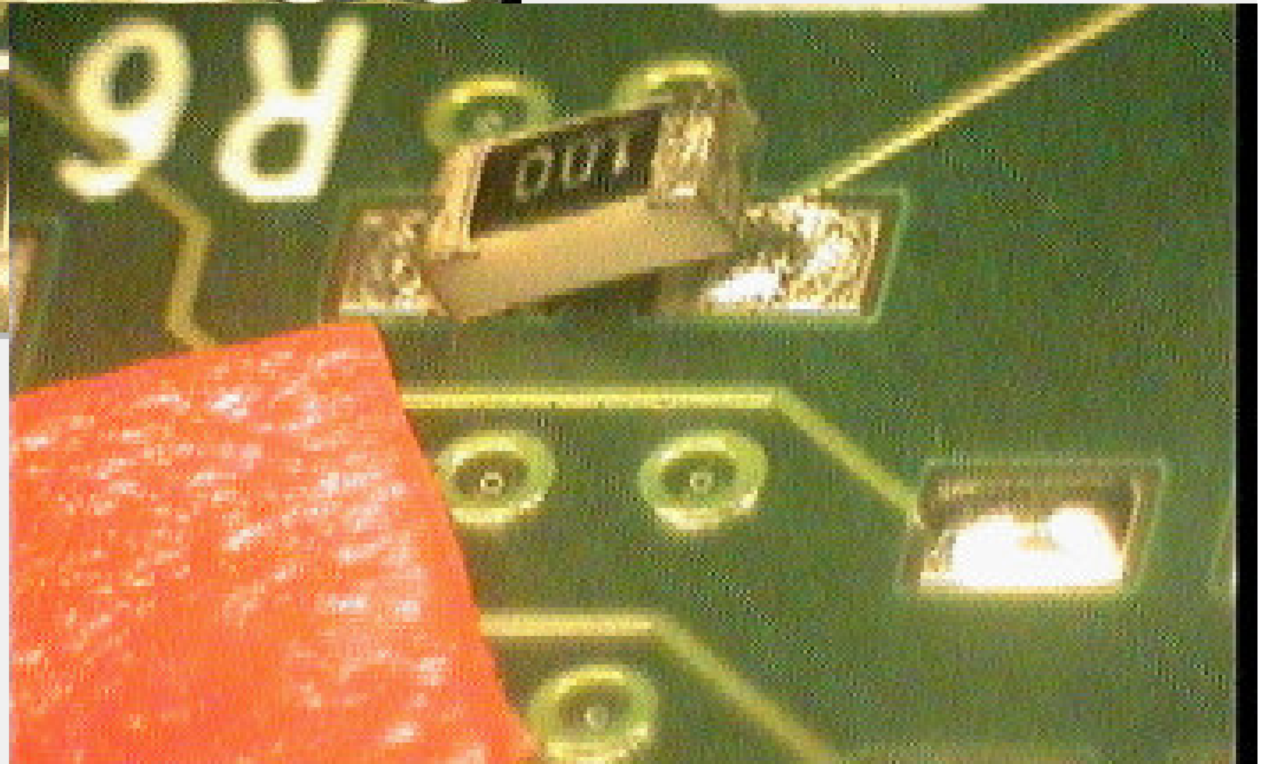




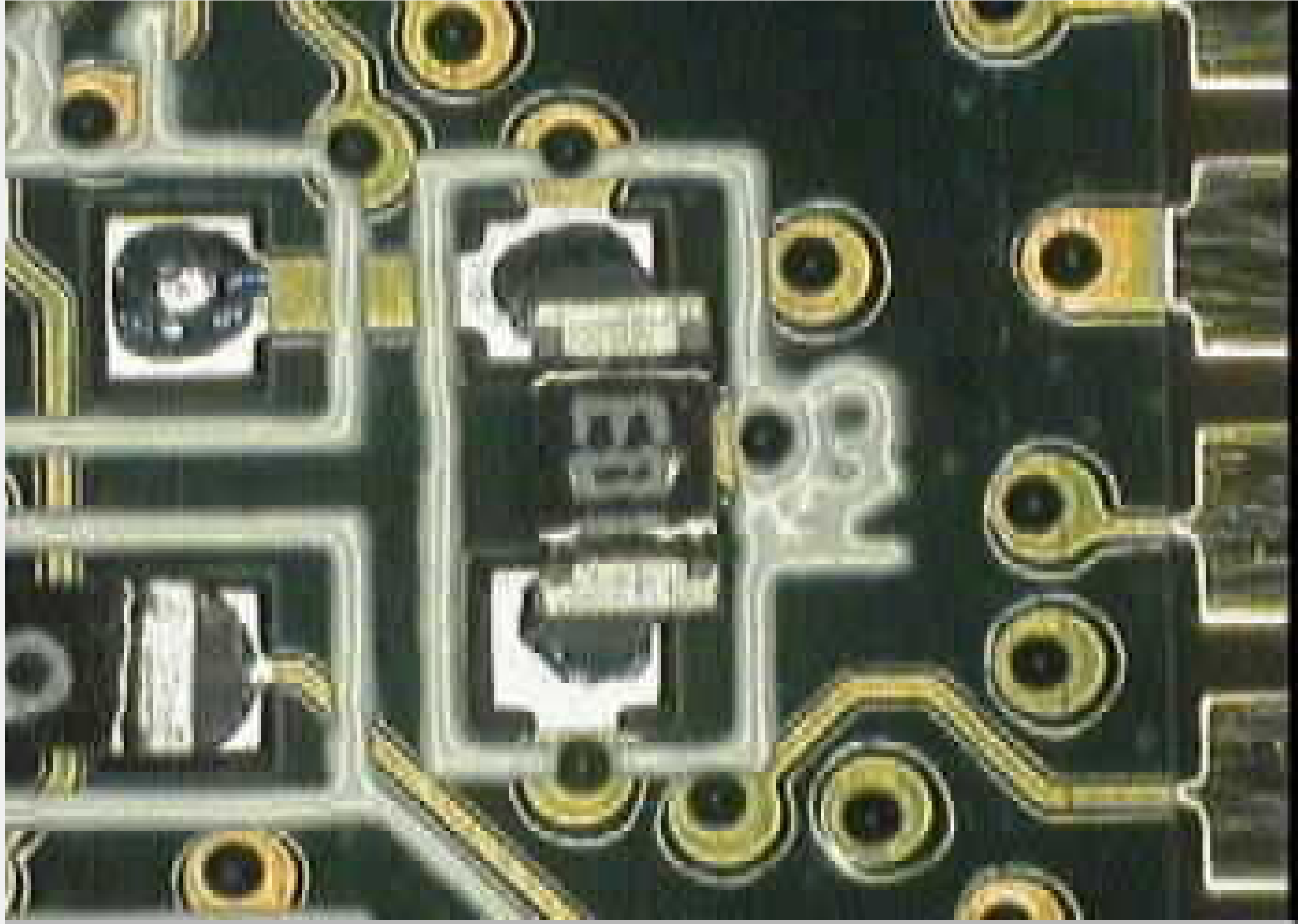


Non-Symmetrical Surface Mount Chip Pads Always results in Tombstoning…



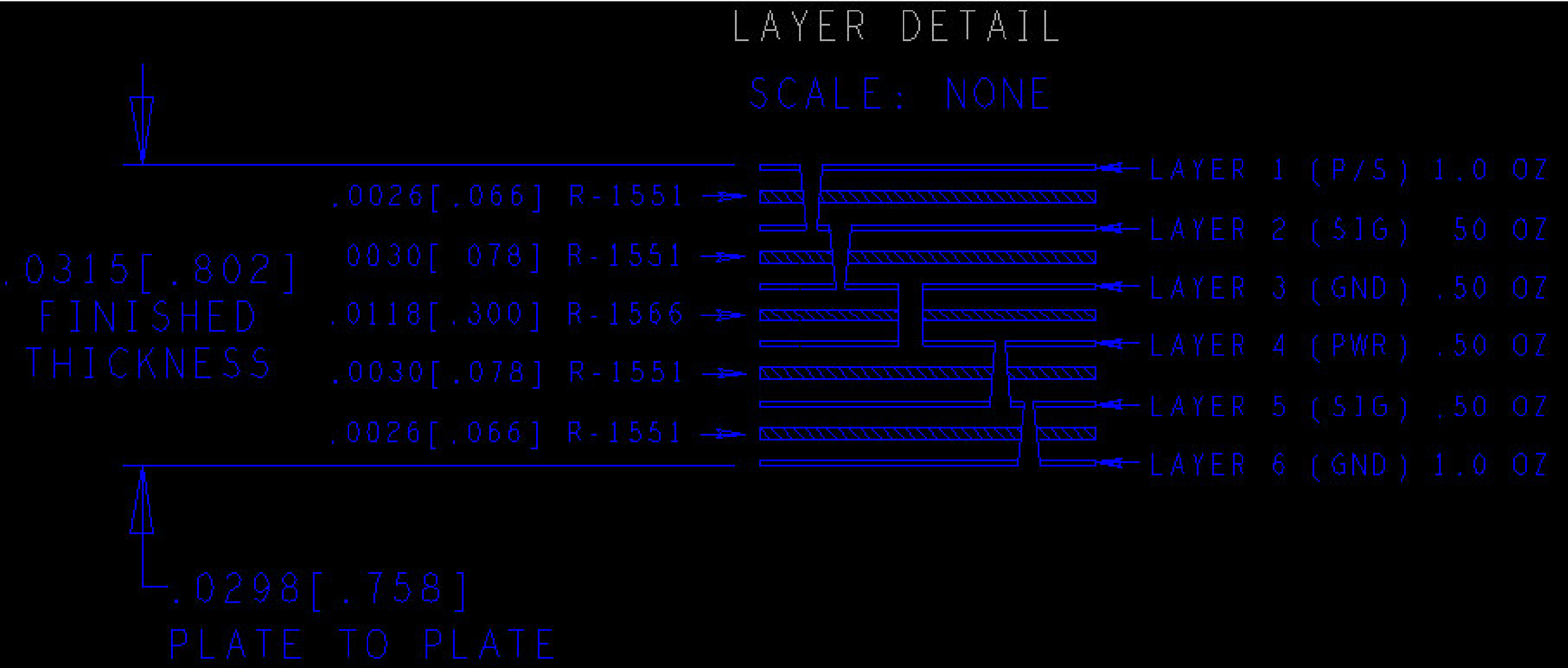


and Mis-Alignment during the reflow process…
especially for the smaller chip devices such as 0603's and 0402's.



Key Issues for Discussion -
(from a designer's perspective)

- **Via – under – BGA**
  - **Micro vias and print specifications**



Key Issues for Discussion -
(from a designer's perspective)

Via Padstack Definitions

Standard Vias

Padstack Name	O/L Pad	Drill	I/L Pad	Antipad	Thermal	Top Mask	Bottom Mask
via018d008	18	8	20	32		-	-
via018d010	18	10	18	34		-	-
via020d010	20	10	22	34		-	-
via022d008	22	8	20	32		-	-
via022d010	22	10	22	34			
via024d012	24	12	24	36		-	-
via025d013	25	13	25	37		-	-
via028d013	28	13	25	37		-	-
via035d015	35	15	27	39	037X025X045X4X006	-	-
via040d020	40	20	32	44		-	-
via045d035	45	35	40	50	065x051x045x4x007		

Notes:

RED	Emmerging Technologies - Fine Pitch BGA, PCBs Less than .062 thickness
GREEN	Standard and Production Technologies - PCBs .062 thru .093 thickness
BLUE	Production Technologies - PCBs .093 thickness or greater

Choose Via to provide for 7.5 or less Hole Aspect Ratio
Hole Aspect Ratio = PCB Thickness / Smallest Finished Hole Diameter

Key Issues for Discussion -
(from a designer's perspective)

Custom Vias

Padstack Name	O/L Pad	Drill	I/L Pad	Antipad	Thermal	Top Mask	Bottom Mask
via024d012-b	24	12	24	36		14	28
via025d013-b	25	13	25	37		15	29
via028d022-b	28	22	34	46		24	32
via035d015-b	35	15	27	39		17	39
via028d013-b	28	13	25	37		15	32
via035d015-m	35	15	27	39		39	39
via040d020-m	40	20	32	44		44	44
via045d035-m	45	35	40	50	065x051x045x4x007	50	50
via025d013-m	25	13	25	37		29	29
via032d013-ttp	32/25	13	25	37		15	36
via032d010-ttp	32/20	10	20	34		12	36
via032d013-btp	25/32	13	25	37		36	15
via032d010-btp	20/32	10	20	34		36	12
via024d012-c	24	12	24	36		14	14
via032d018-c	32/35 (T/B)	18	30	42		20	39
via025d016-c	21/25	16	25	31		18	29
via026d017-c	22/25	17	26	32		19	30

Notes:

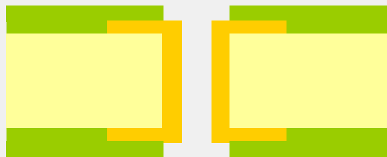
<dash> B	S/M open on bottom side pad
<dash> T	S/M open on top side pad
<dash> M	S/M open on both side pads
<dash> TTP	Top Testpoints only - see definition
<dash> BTP	Bottom Testpoints only - see definition
<dash> C	Custom - see definition

Key Issues for Discussion - (from a fabrication perspective)

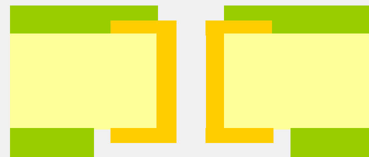
- **Via – under – BGA** (soldermask "via-capping" solutions; hole-plugging do's and don'ts)

Via Plugging Approaches

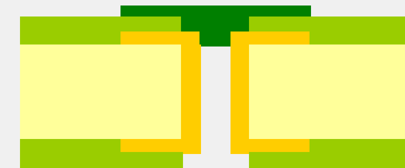
("Protected Vias" per IPC-SM-840C)



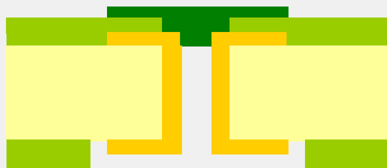
#1
Encroachment to Via Approach
(aka, tentbust, rimless vias, gas holes)



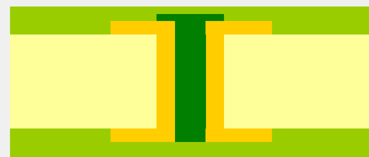
#2
Encroachment to Via Approach
(For Test Point Access on Bottom Side)



#3
PostPlugged Via Approach
(aka, capped, plugged vias)
(Bottomside "Encroachment")
(Via Plugging is 0 - 50% of the hole)
(With ~95% of Vias on the Panel Plugged)



#4
PostPlugged Via Approach
(For Test Point Access on Bottom Side)



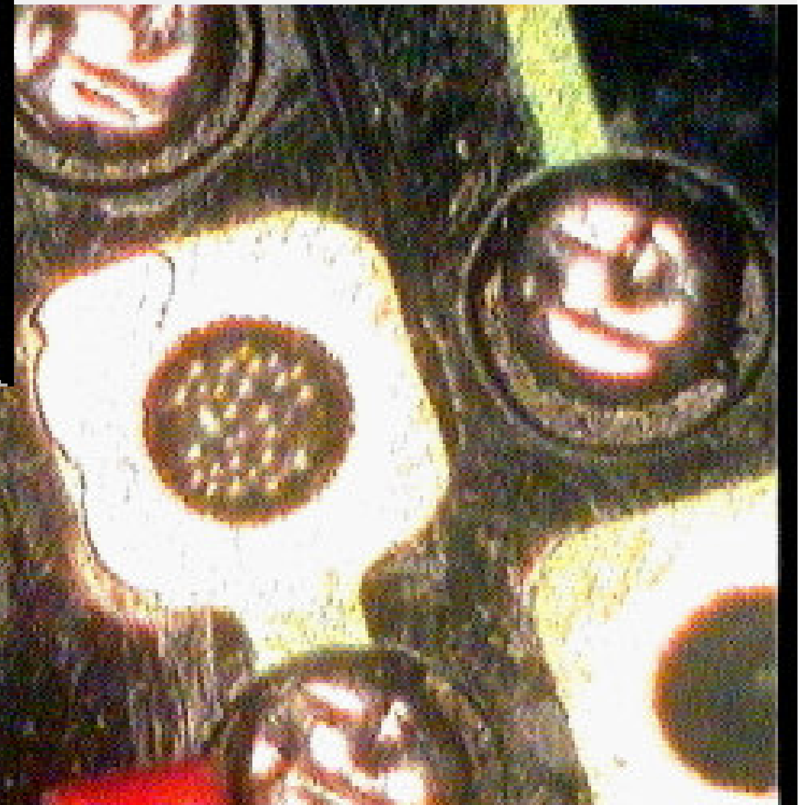
#5
PrePlugged Via Approach
(Via Plugging is 80 - 100% of the hole)

Key Issues for Discussion - (from a assembly perspective)

- **Via – under – BGA** (soldermask "via-capping"…Why it's a must!)

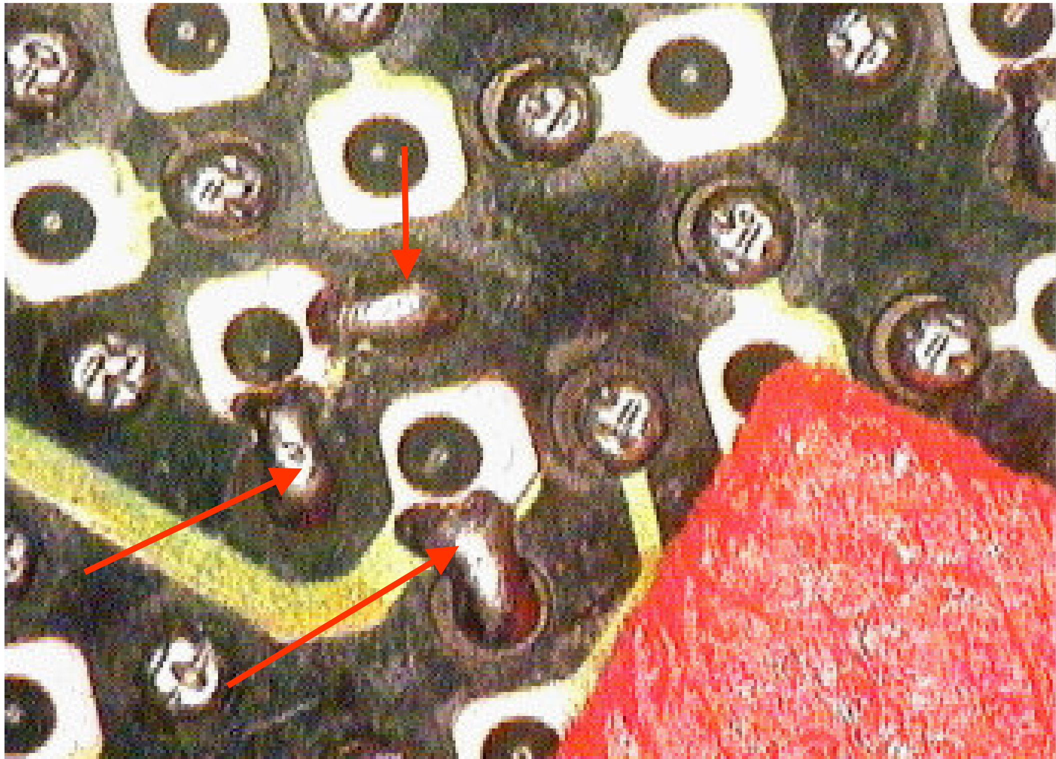
Solder Paste Solder Spheres fill an unmasked via during the screen print process.

Photo at 75X mag



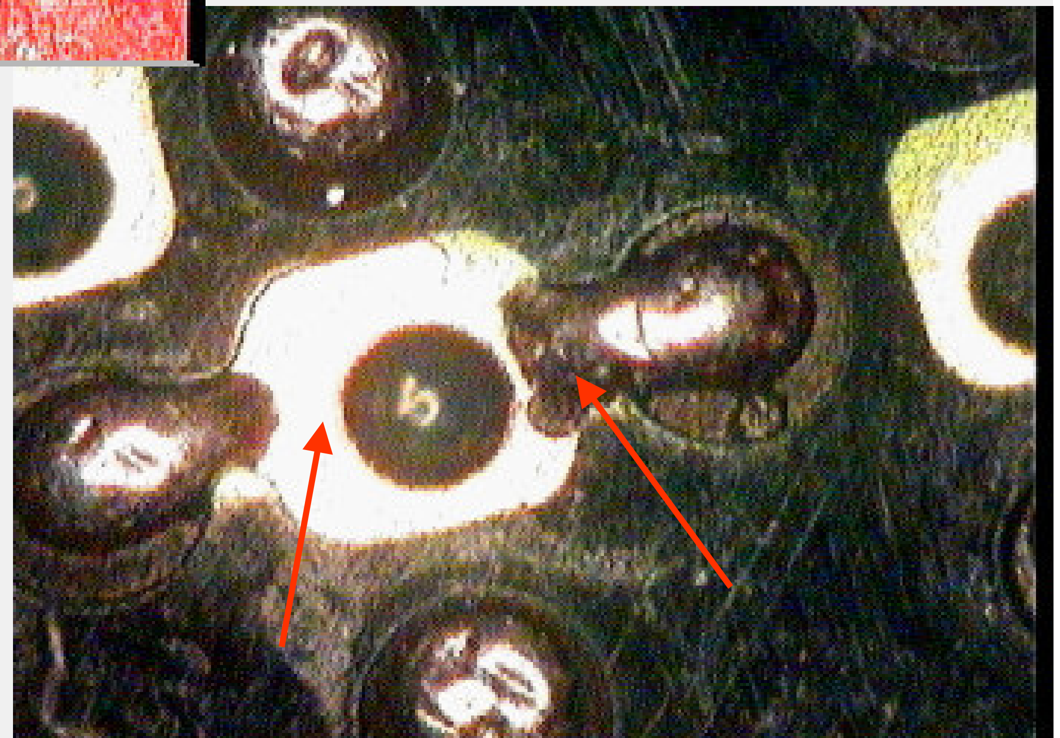
Solder Paste Solder Spheres filling an unmasked via during the screen print process is unavoidable!

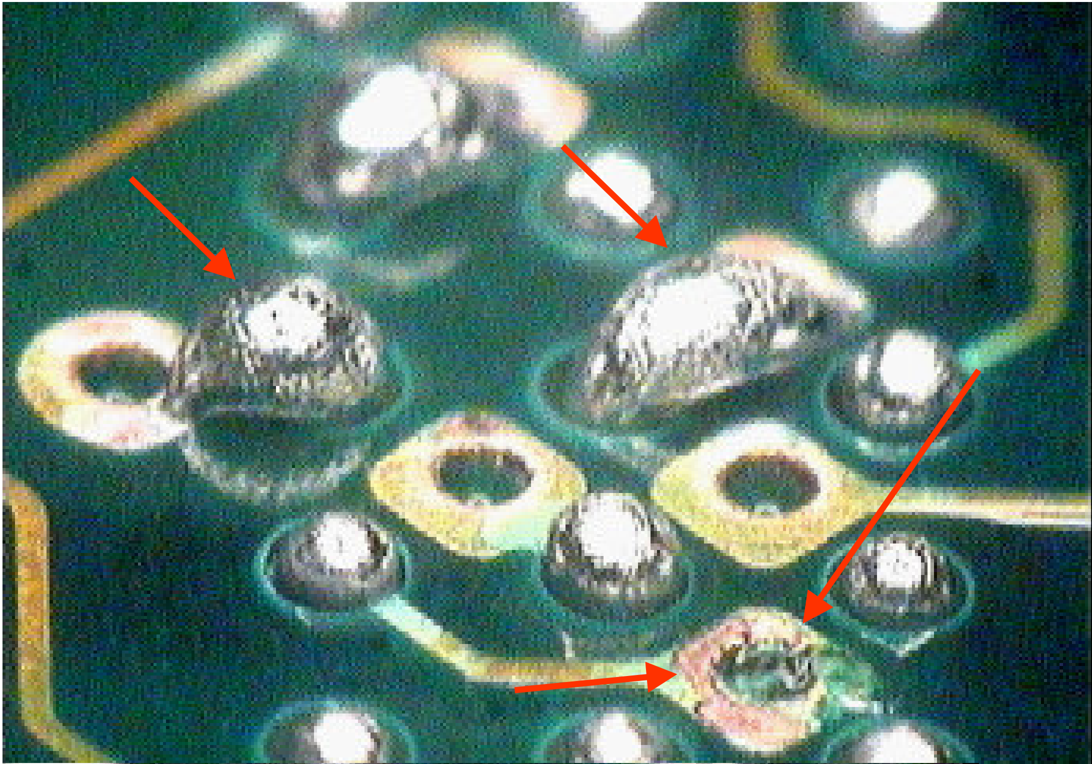
Photo at 150X mag



When Solder Paste Solder Spheres fill an unmasked via (during the screen print process) it results in Solder Shorts to Non-Common Conductors.

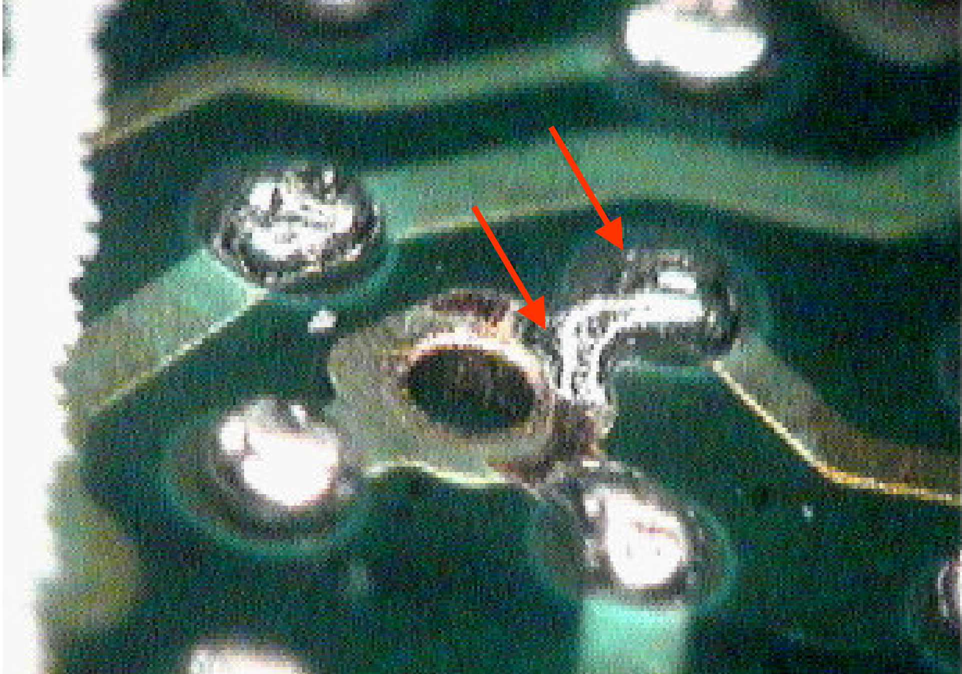
Solder Shorts to Non-Common Conductors from solder paste filling unmasked via's is unavoidable!

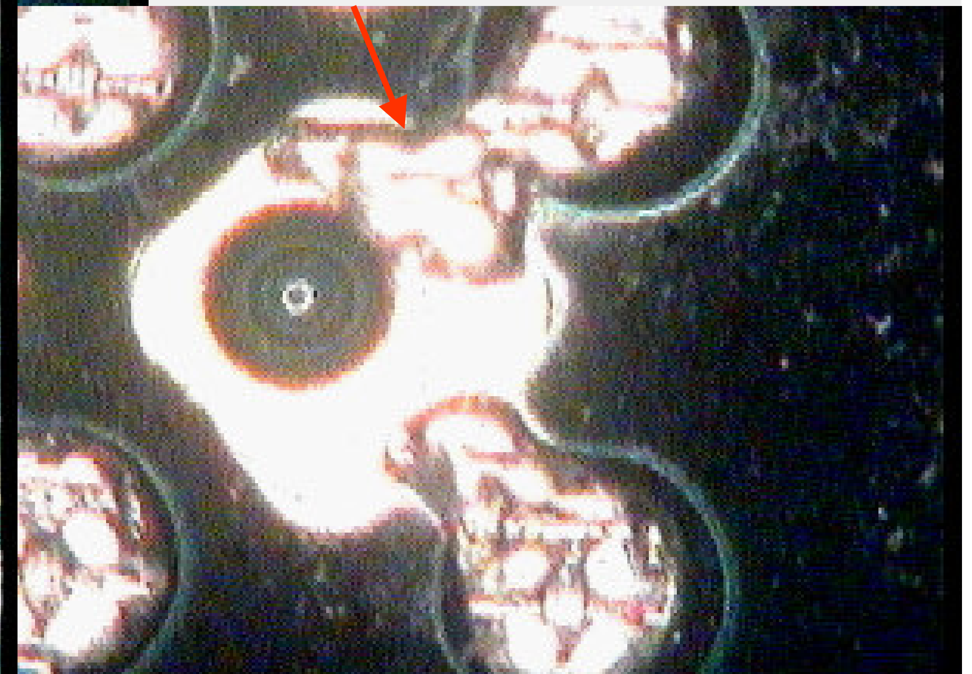




Solder flows to the place of least resistance (the hottest place).

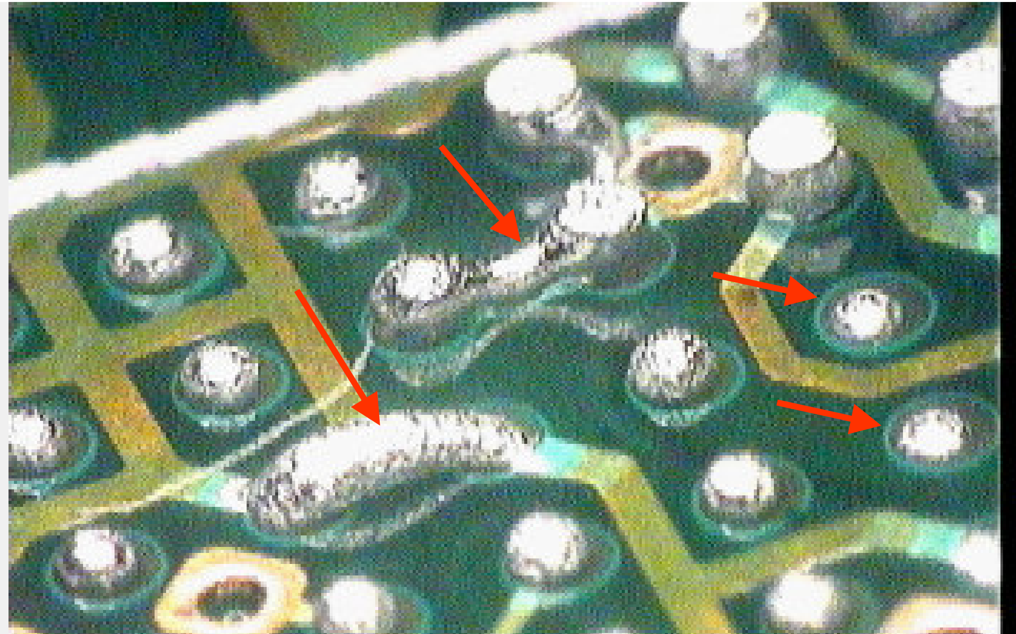
An improperly capped Via is hotter than a pad and will always suck solder from surrounding pads causing shorts and solder scavenging!

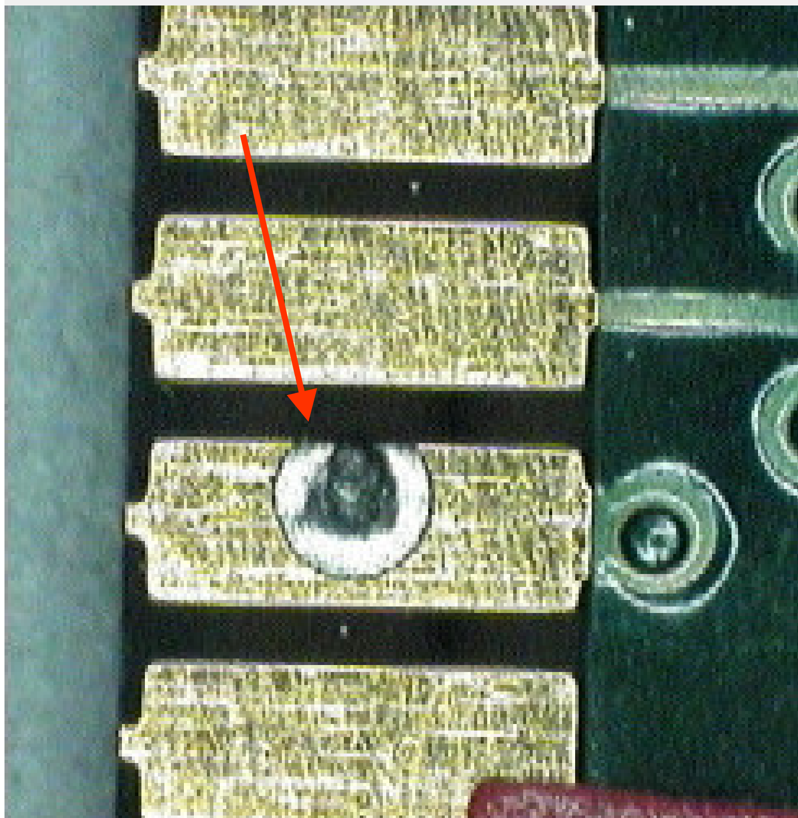


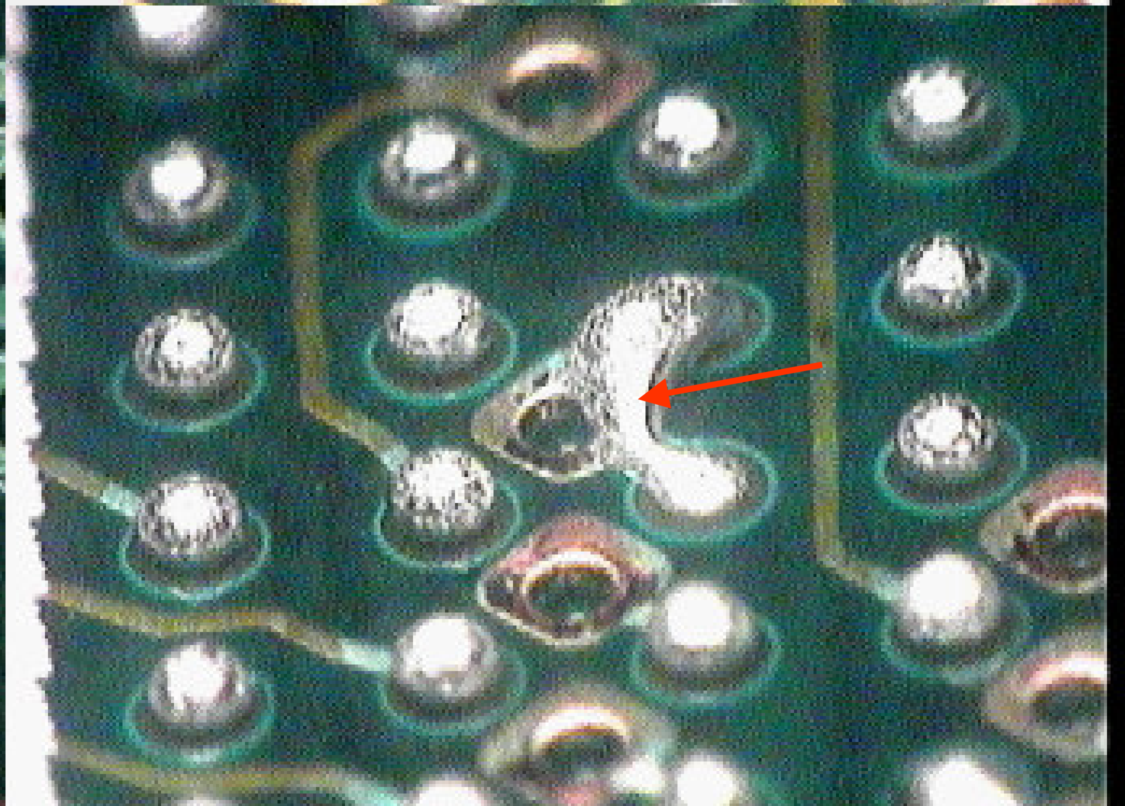


Improper Capping of Via's leads to out gassing of the solder trapped in the Via during normal convection reflow processing.

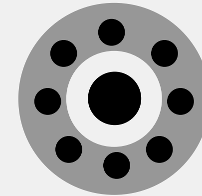
Out gassing of solder will always result in shorts, opens, insufficient, and solder splatter on gold fingers!





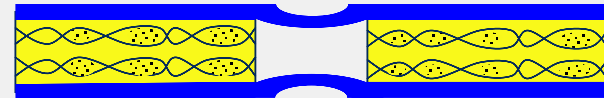


Key Issues for Discussion - (from a fabrication perspective)



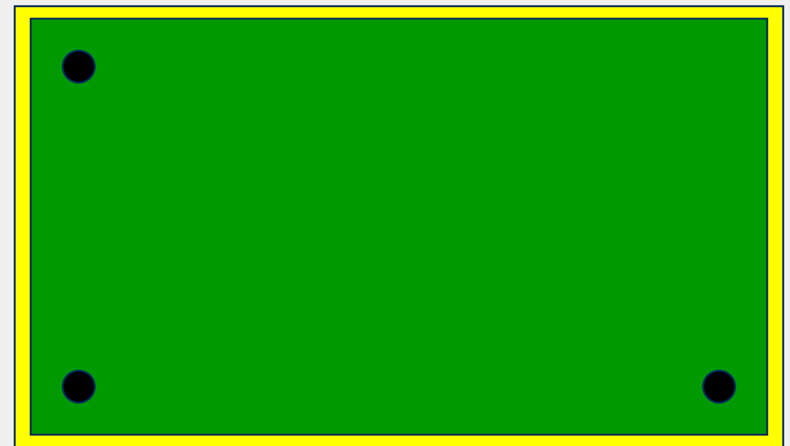
Non-Plated Holes (traps and tricks)

- Metal pads on outerlayers
  - Tenting for fab processing
    - Metal relief around NPTHs
    - Hole size – too big / broken tents
    - Larger sizes are typically routed
    - Best if there's no metal pad on outerlayers



Photoresist covered Non Plated Holes - Tented

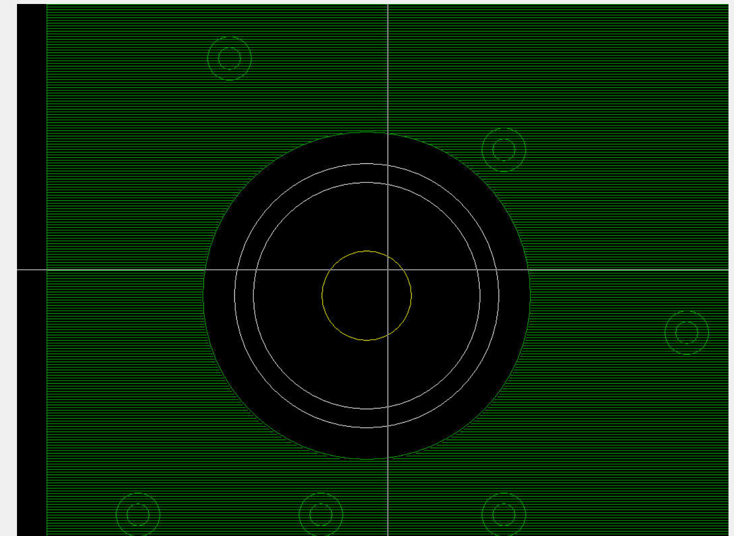
  - Tooling holes for routing
    - Typical sizes are .062", .093", .125"
    - 3 are preferred for orientation
  - Tooling holes for mounting
    - Typically used for screw mounts
    - Metalization final finish concerns

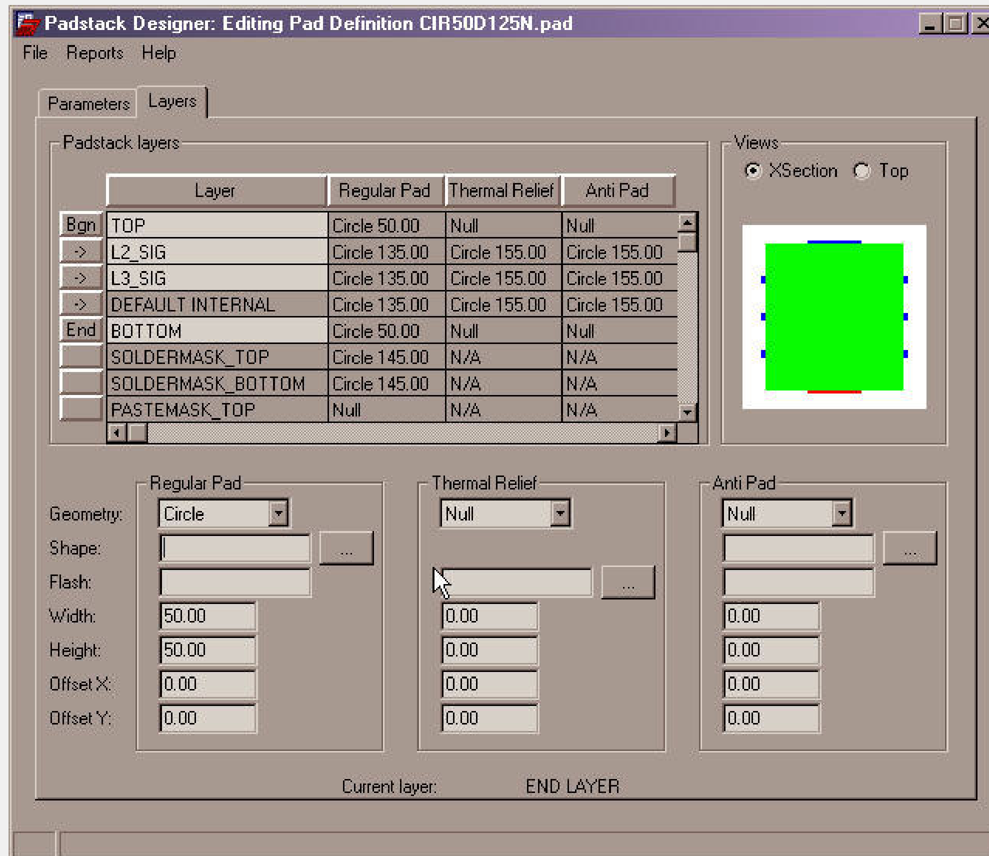


Key Issues for Discussion - (from a designer's perspective)

❑Non-Plated Holes (traps and tricks)

•Metal pads on outerlayers



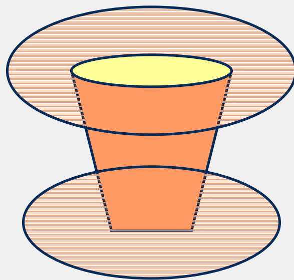


Key Issues for Discussion - (from a fabrication perspective)

- **Vias** (Aspect ratio challenges; pad size choices)

Laser Drilled Microvia Hole

Capture Pad

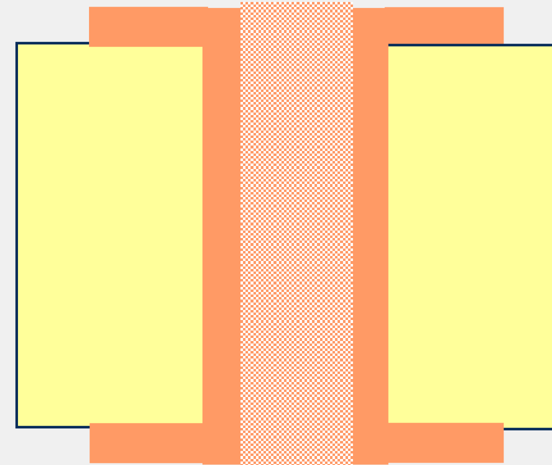


Target Pad

Typical Geometry's

Drilled Hole Size - ~ .006" dia.
Target Pad Size - ~ .012" dia.
Capture Pad Size - ~ 80% the solderball size
Aspect Ratio - <= .7 : 1

Mechanical Drilled Through Hole (Comparison)



Typical Geometry's

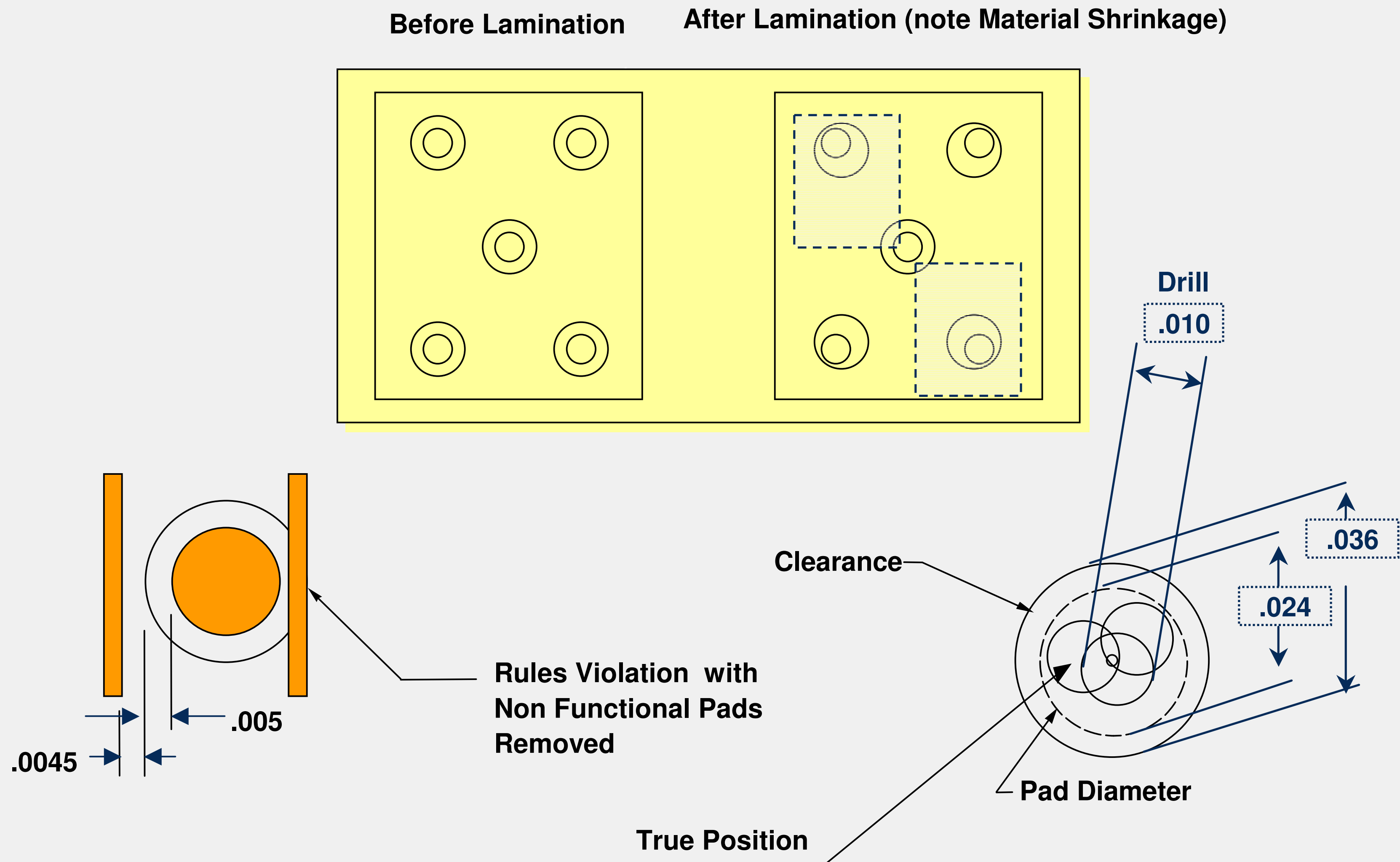
Drilled Hole Size - ~ .010" dia.
Pad Size - ~ .024" dia.

Aspect Ratio - <= 8.9 : 1

Key Issues for Discussion - (from a fabrication perspective)

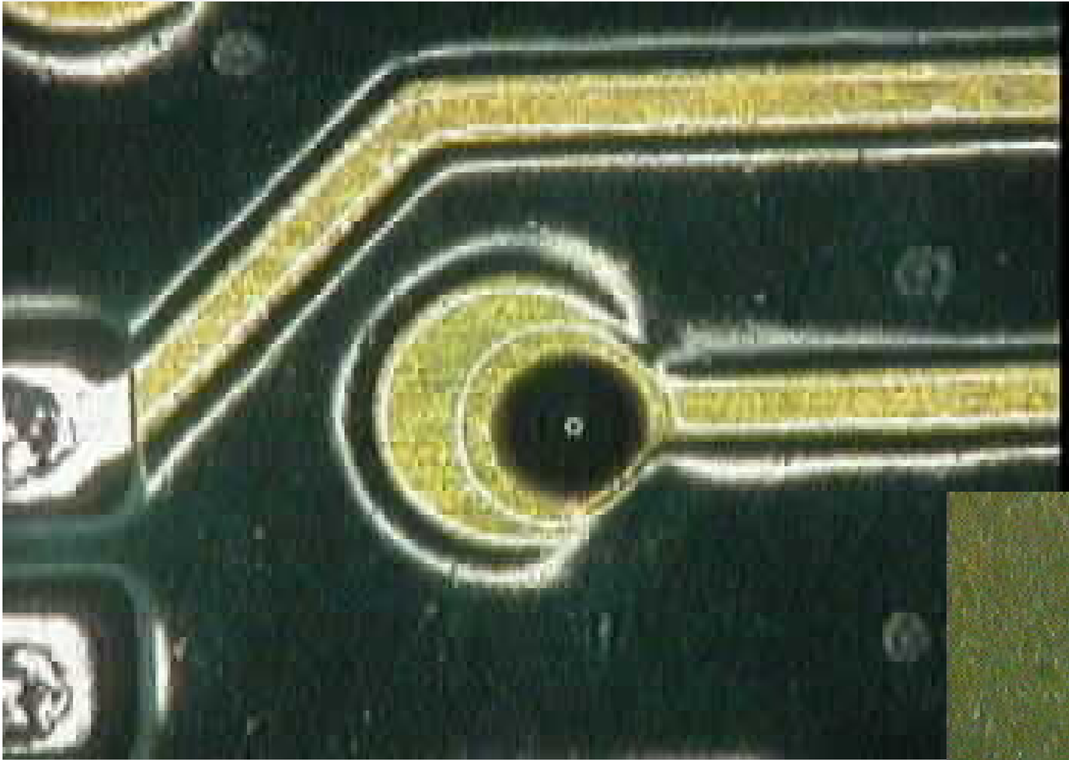
•Vias – Why do we need the larger pad sizes?

LAMINATE / DIMENSIONAL STABILITY



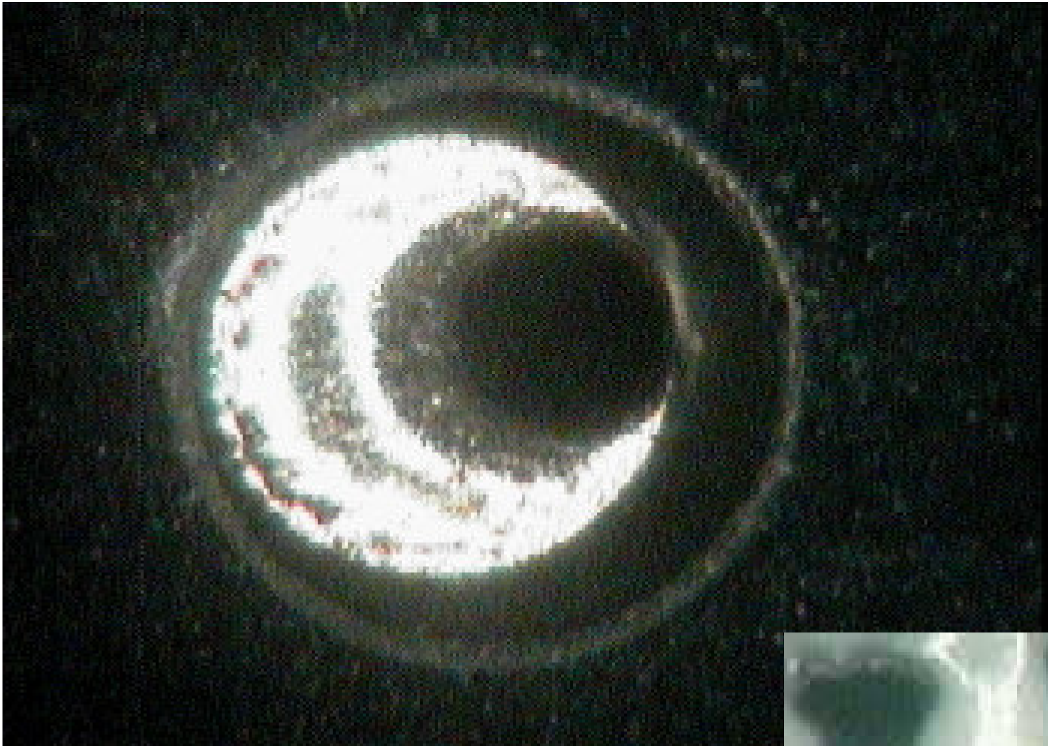
Key Issues for Discussion - (from a assembly perspective)

- **Vias – Why do we need the larger pad sizes?**

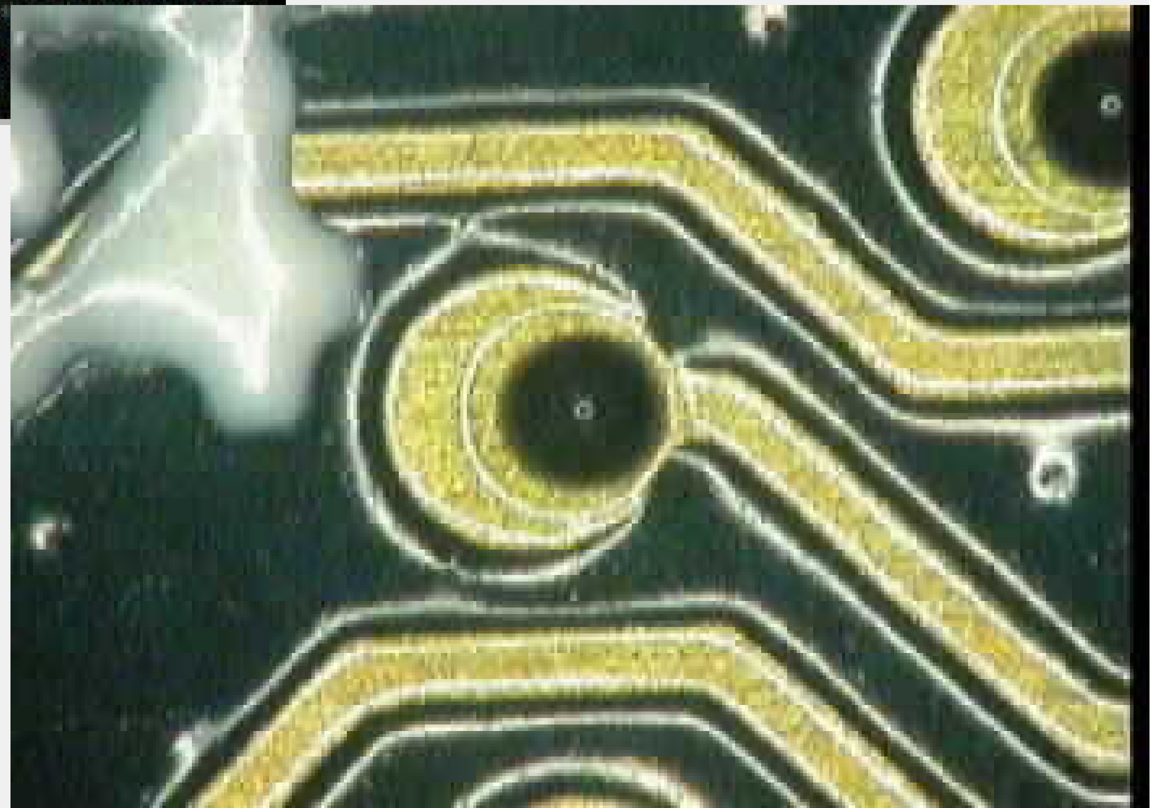


To Ensure Quality PCB's…

are received!



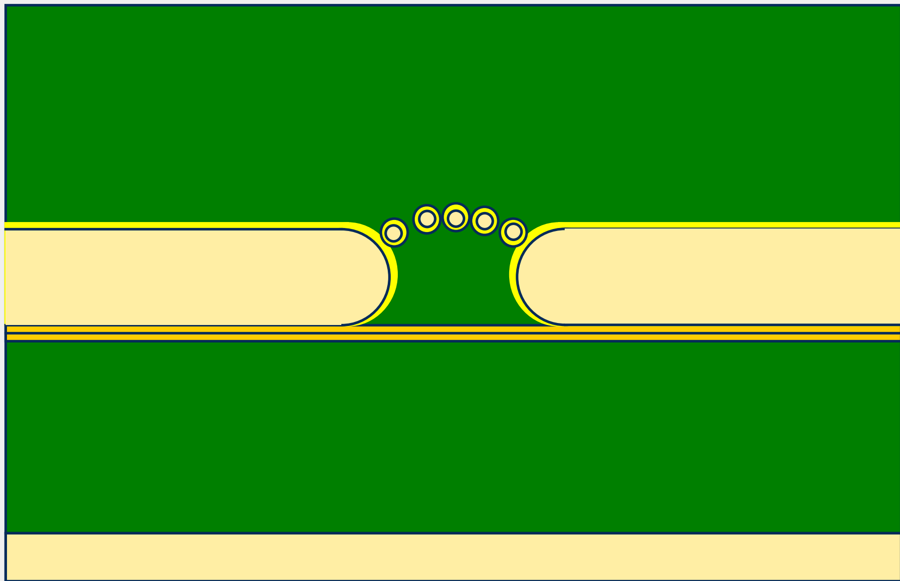
When Quality PCB's are not received…

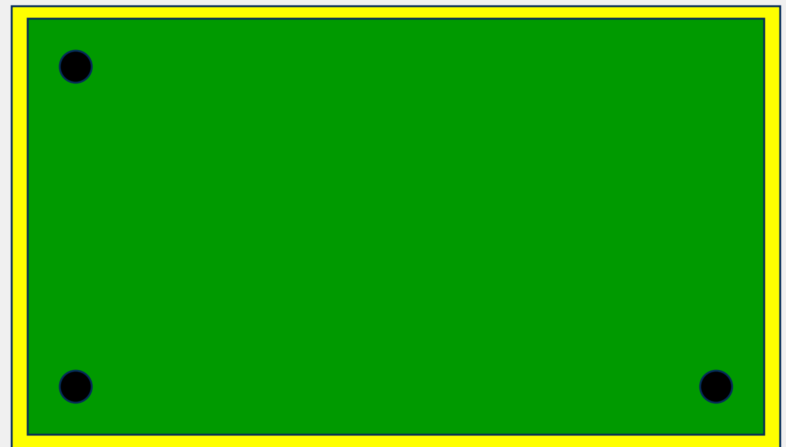


on time Delivery is nearly impossible!

Key Issues for Discussion - (from a fabrication perspective)

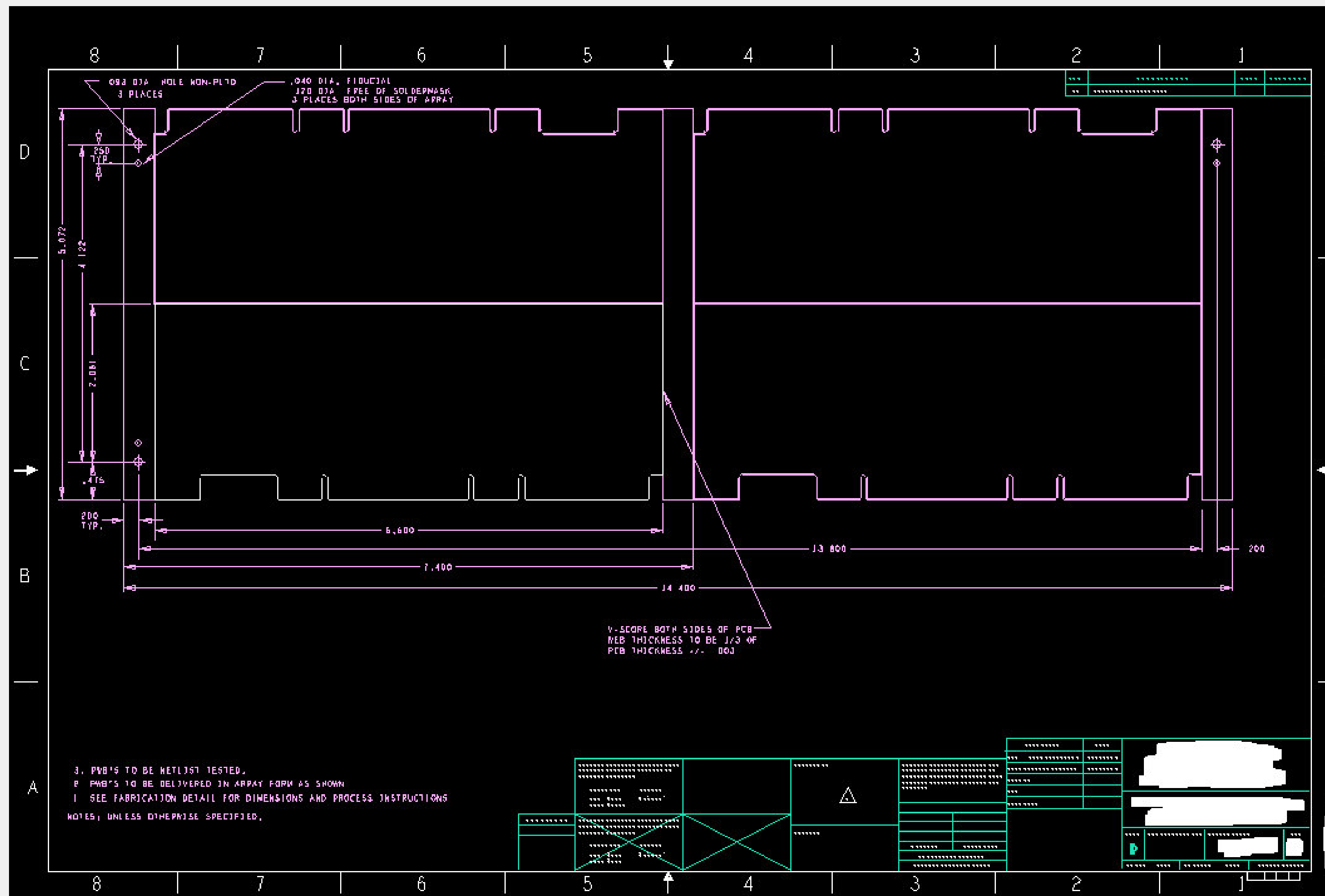
- **Proper Soldermask Approaches** (why it's important on those "rat-bites" too)
  - Soldermask should be relieved from PCB edges, NPTHs, scorelines, c'bore/c'snks, and cutouts.
    (to minimize the possibility of chipping or ragged edges)



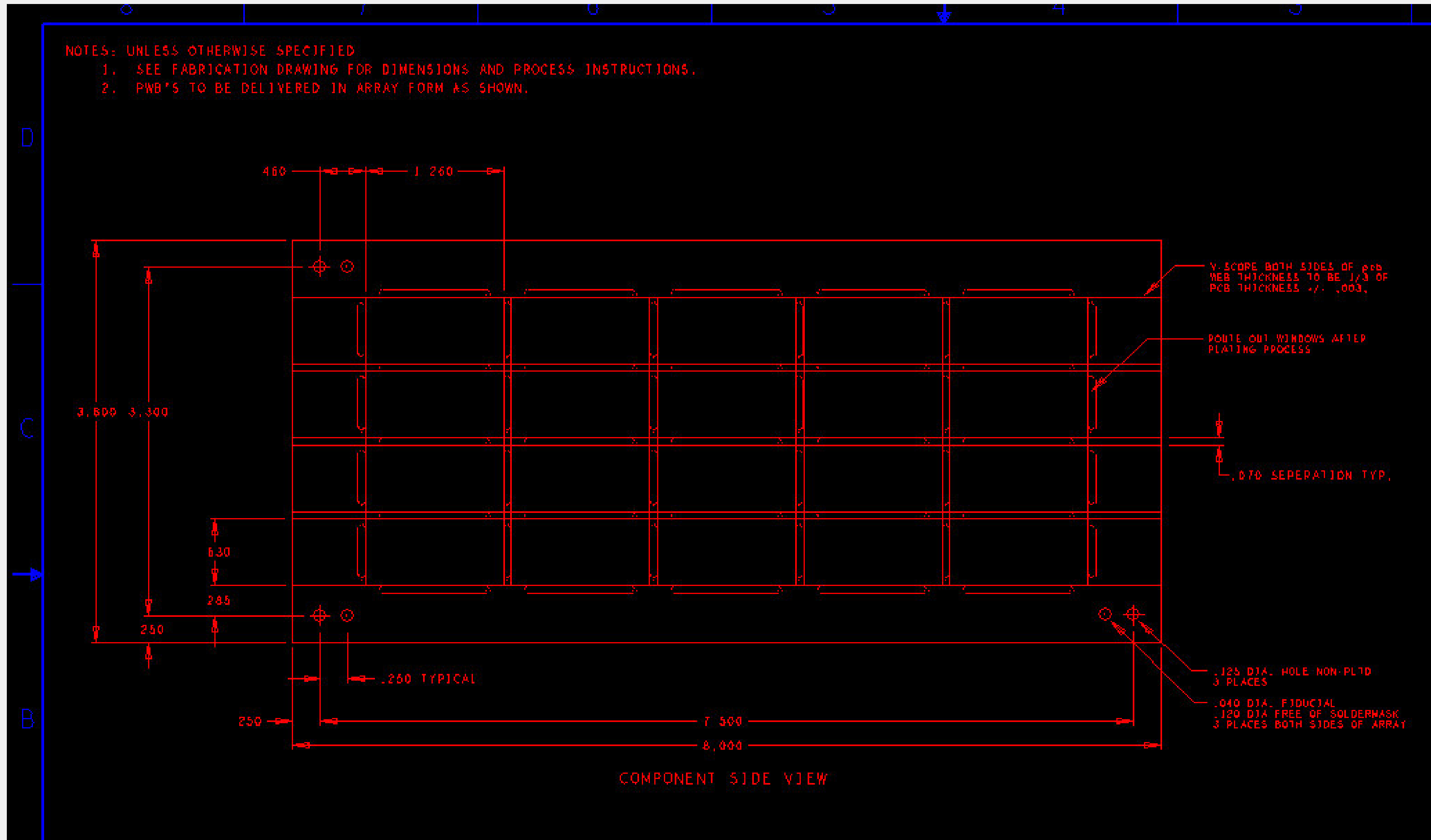


Key Issues for Discussion - (from a designer's perspective)

- Proper Array Dimensioning



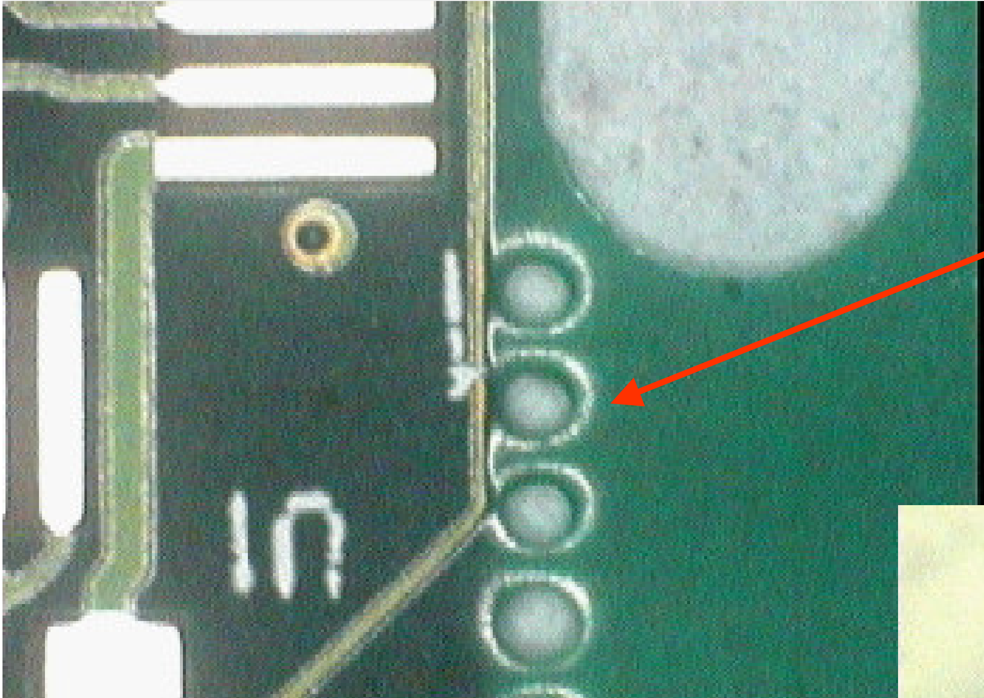
Key Issues for Discussion - (from a designer's perspective)



- Proper Array Dimensioning - Continued

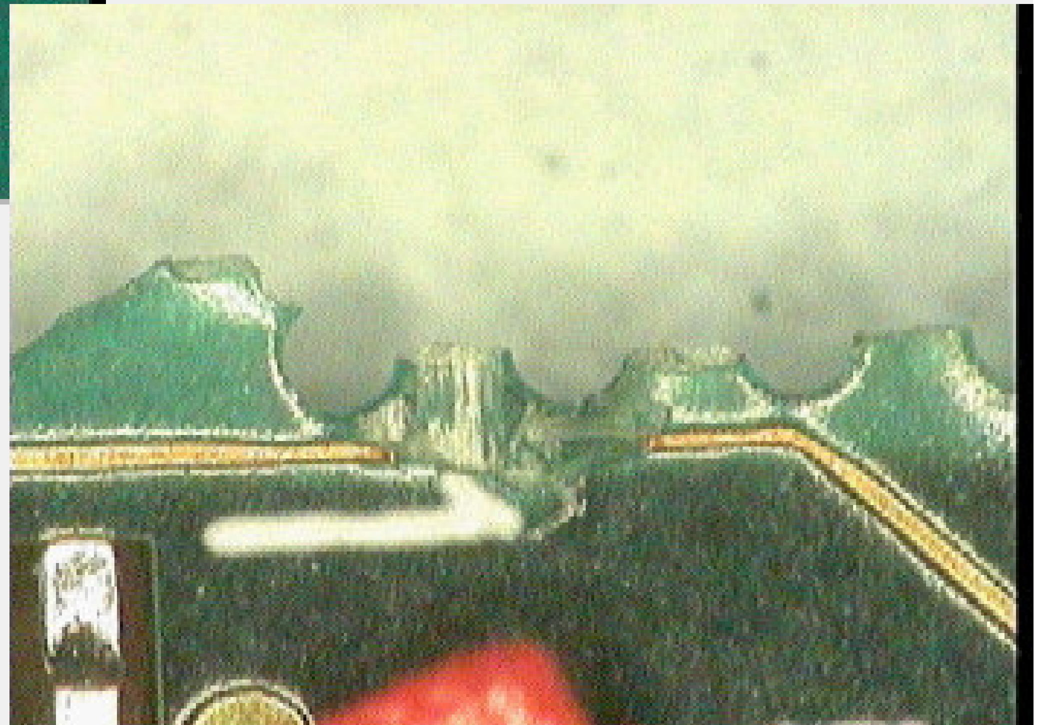
Key Issues for Discussion - (from a assembly perspective)

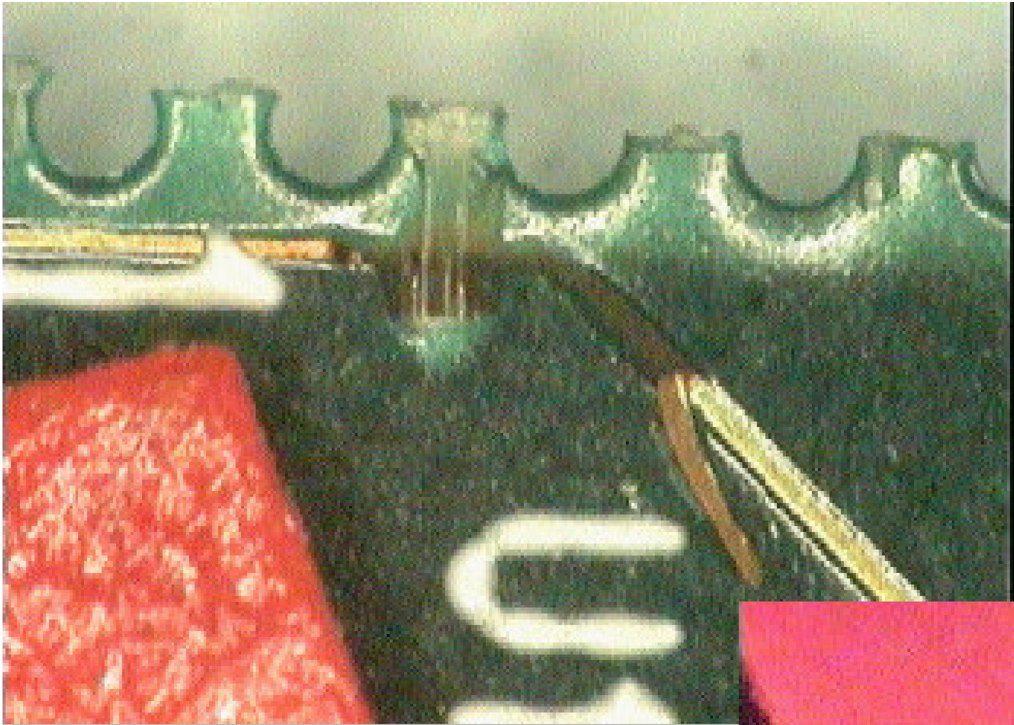
- **Proper Soldermask Approaches** (why it's important on those "rat-bites" too)



Solder Mask not Properly Relieved from "Rat Bite" areas always results in…

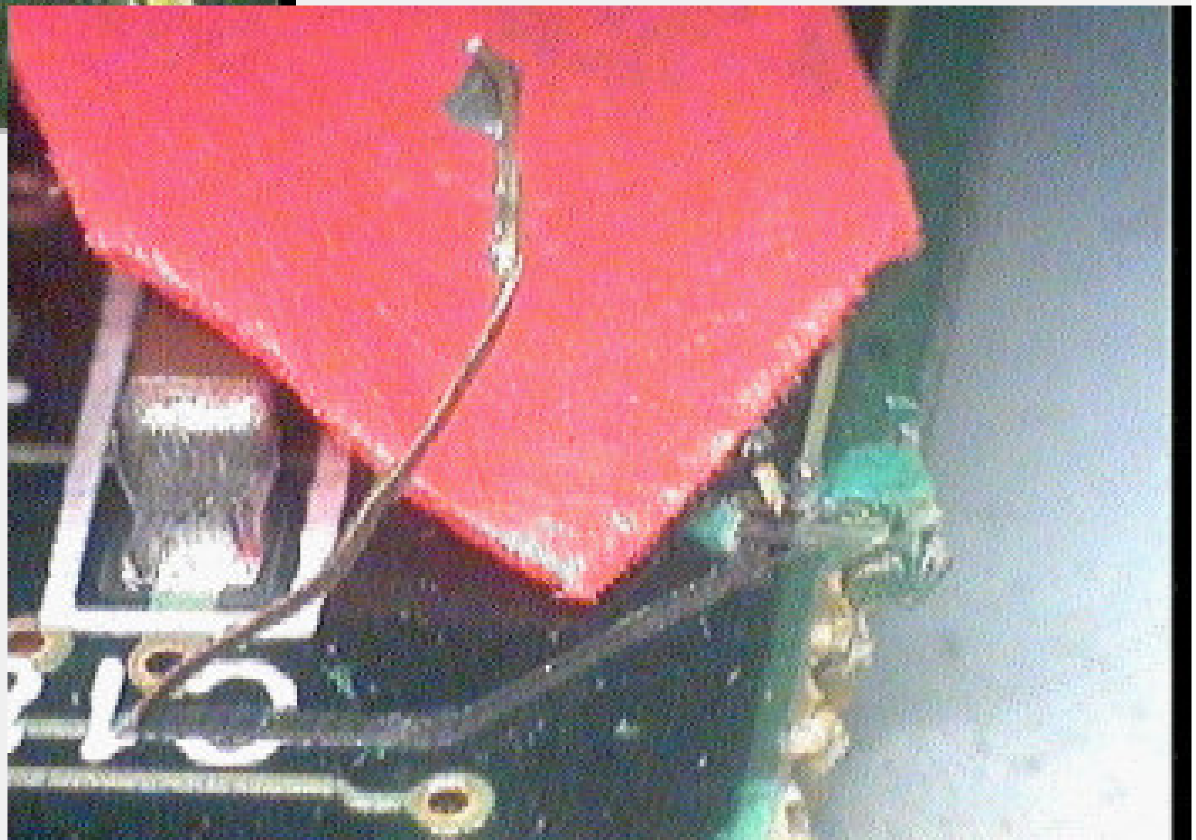
Missing,





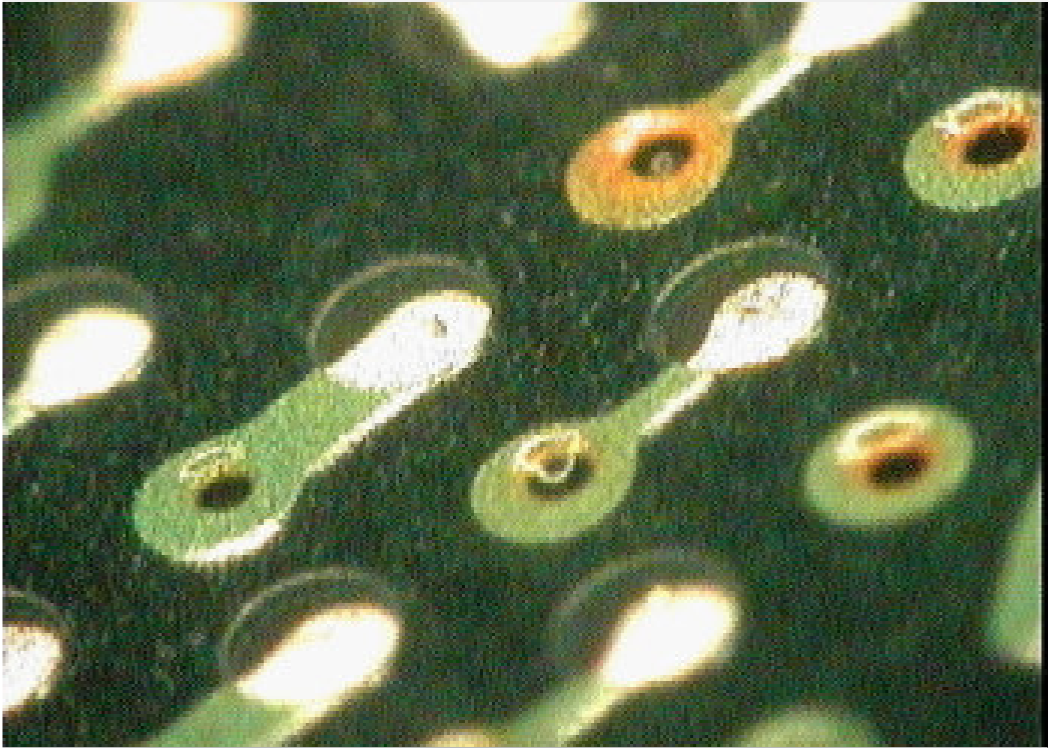
Torn and…

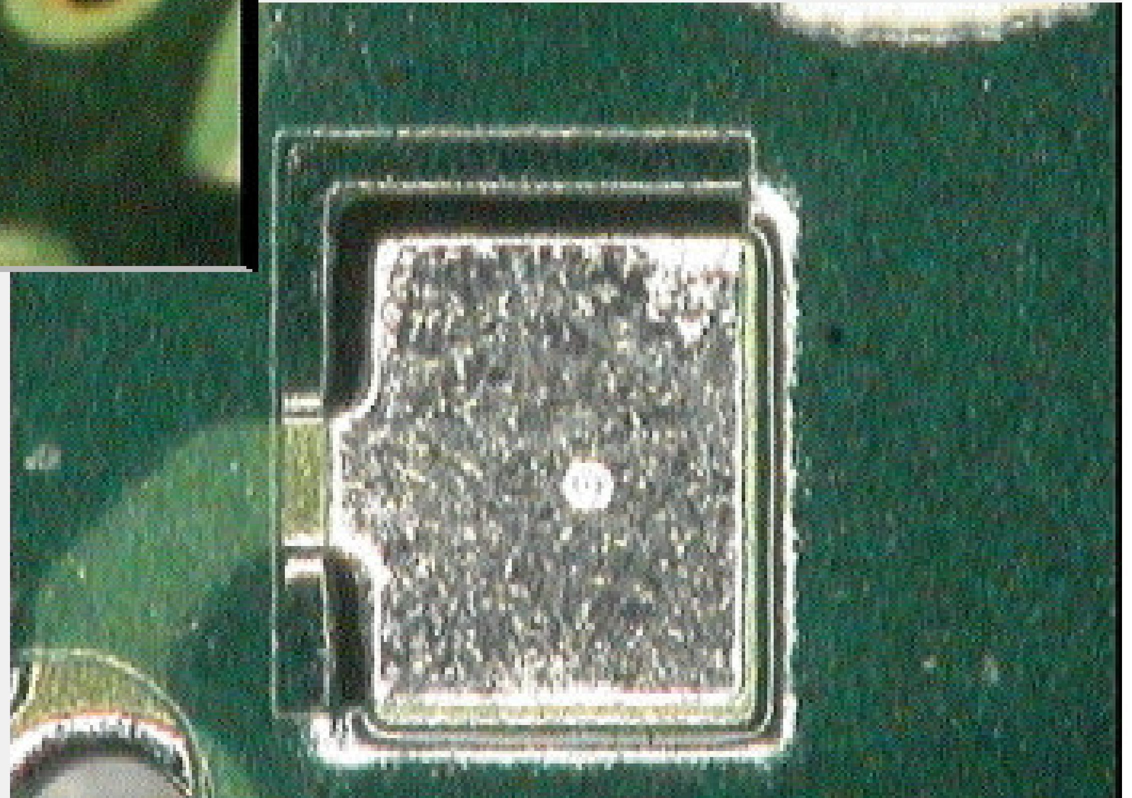
Lifted Traces!



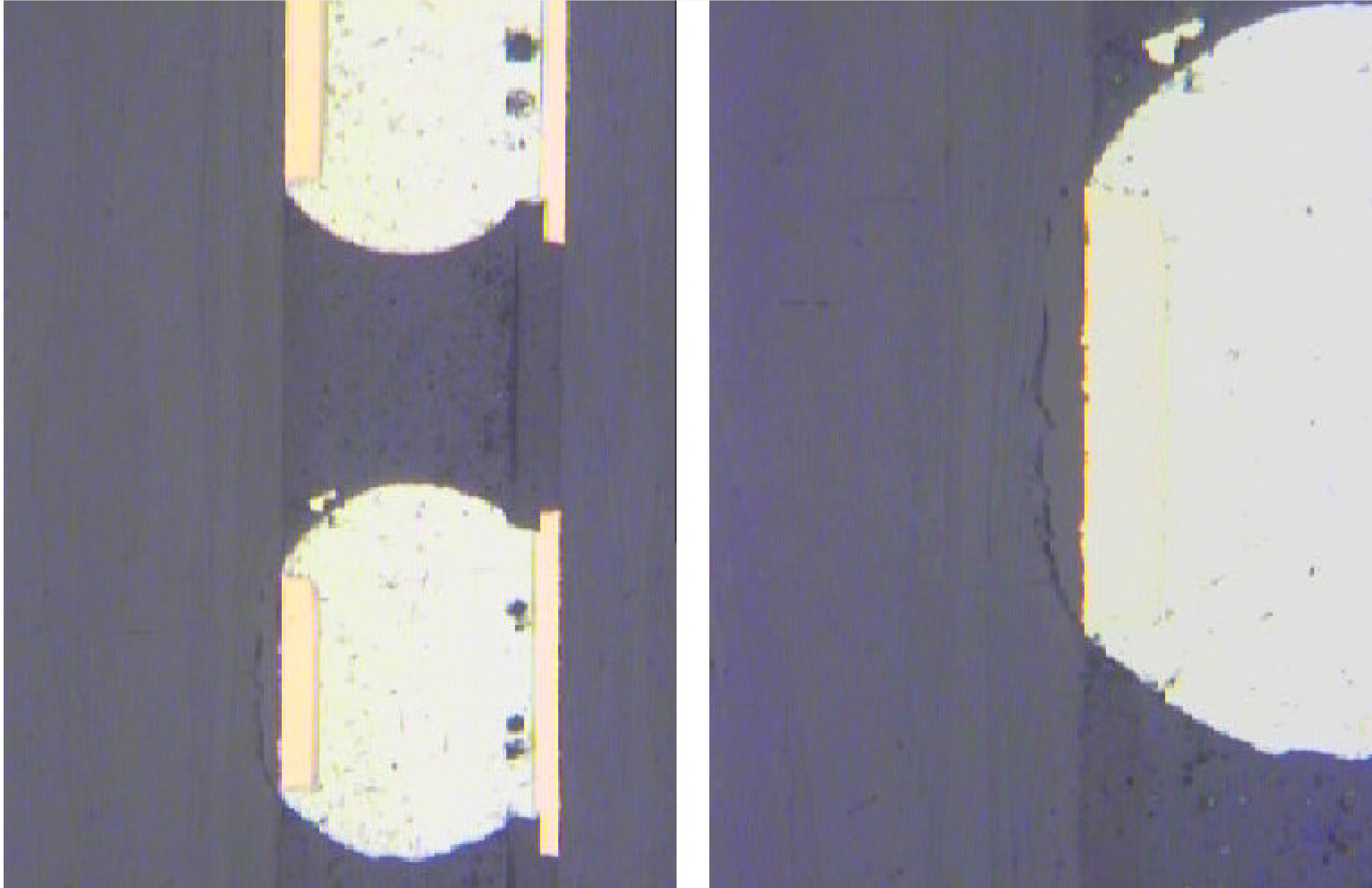
Soldermask not properly relieved from PCB edges, NPTHs, scorelines, c'bore/c'snks, and cutouts always results in chipping or ragged edges!

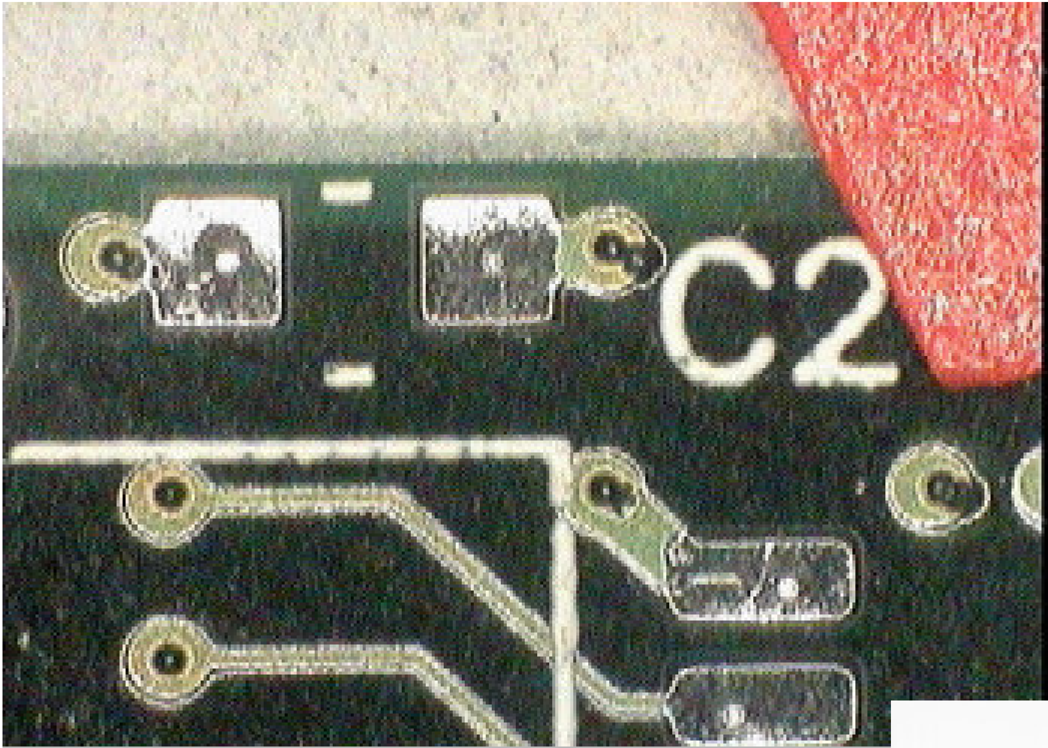
Solder Mask should be sufficiently relieved around all pads, so as to allow for good mask Alignment. Especially BGA pads!





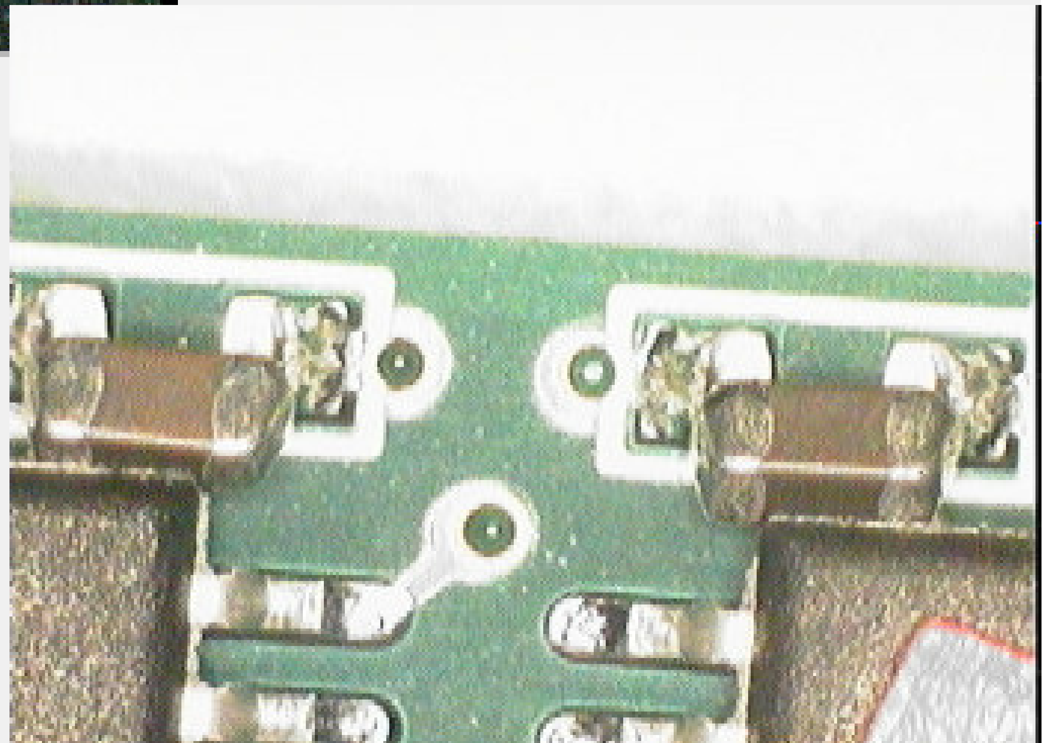
Solder mask that is not properly relieved can result in poor solder connections and CTE Issues take over.



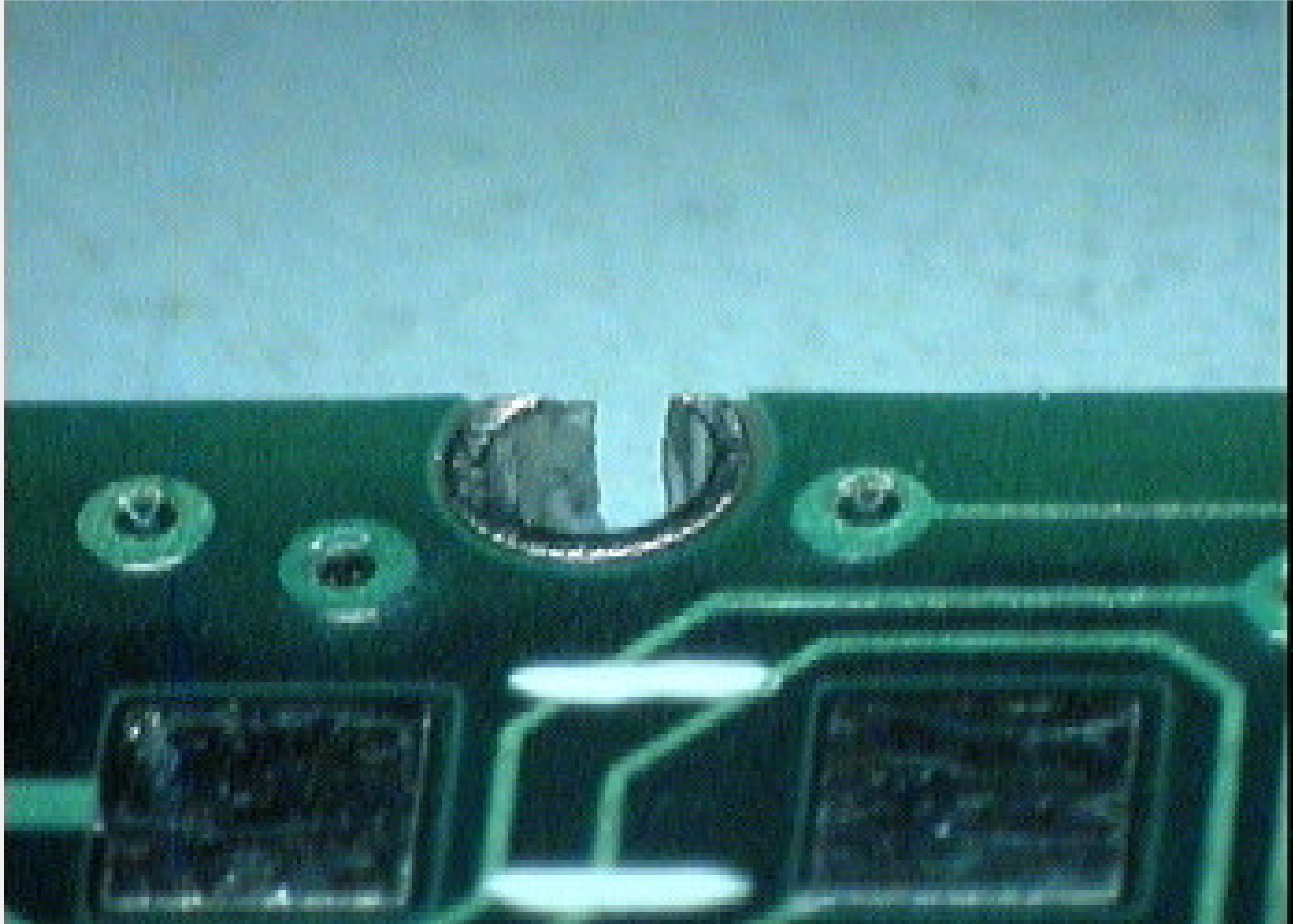


Improperly relieving from PCB edges for Components always results in…

chipping or damaged components.

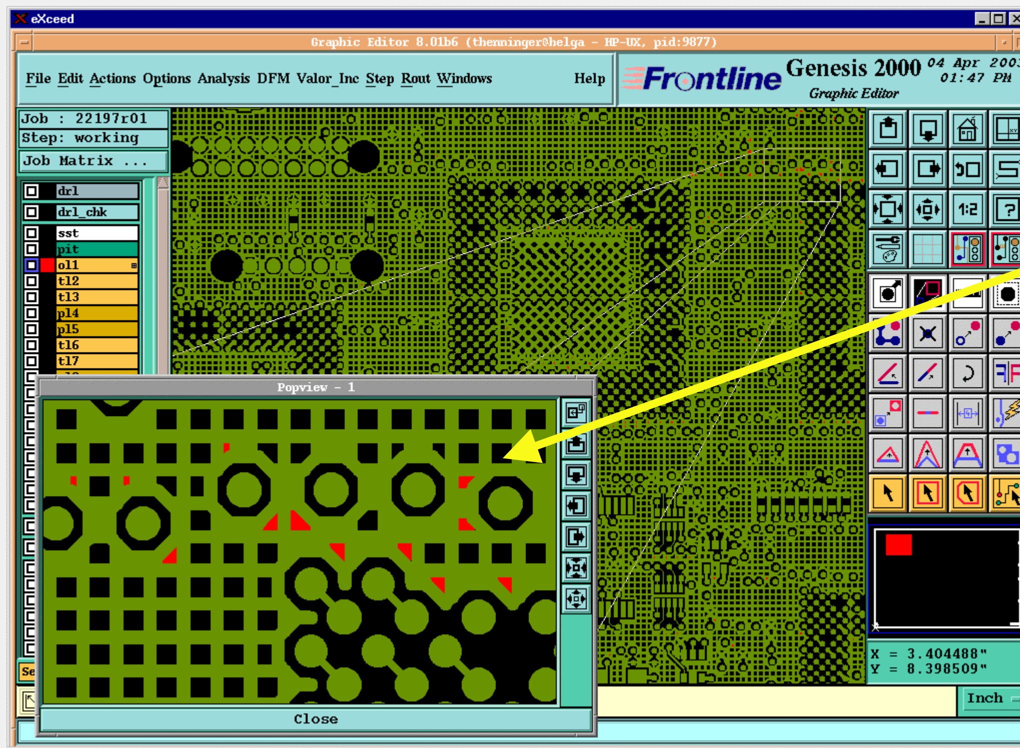


Improperly relieving from PCB edges for Via's always results in damaged via's.

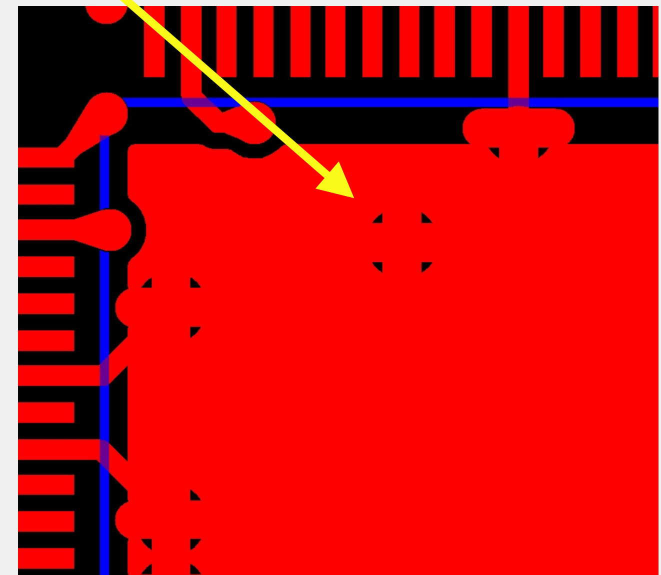


Key Issues for Discussion - (from a fabrication perspective)

- **Planes and thermals** (how a little heat can make a fabricator soar)



Each small "sliver" of photoresist can redeposit on the layer and cause an open or a short (depending on where it lands).



Reasons not to use crosshatch thieving