Hallmark Circuits, Inc.

Controlled Impedance

from the fabricators view

Rick Norfolk

Outline

- What is Impedance?
- Types of constructions
- Impedance factors
- Importance of dielectric thickness and line width
- TDR Measurement
- More Information

Presentation Legend

- For the purposes of this presentation we shall use orange color as “copper” and yellow color as “dielectric.”

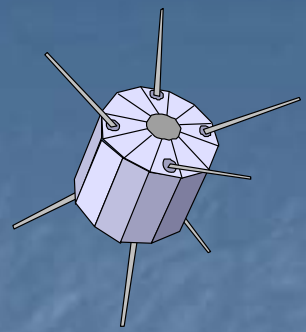
COPPER

DIELECTRIC

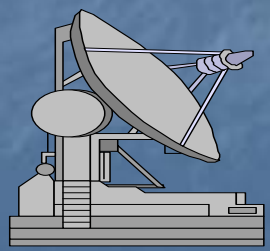
What is Characteristic Impedance?

- Definition of terms - IPC D 317 Design Guidelines
- Characteristic impedance - The resistance in parallel circuits and power planes to the flow of alternating current.
- Measured in ohms as in direct current but this is an alternating current field effect.

Why is it needed?



- High speed signal transmission
- Propagation delay, high frequency component
- Energy stored in fields in inner and outer space - conductors define fields
- Impedance is the square root of the ratio of inductance to capacitance
- High speed chips, telecom, microwave



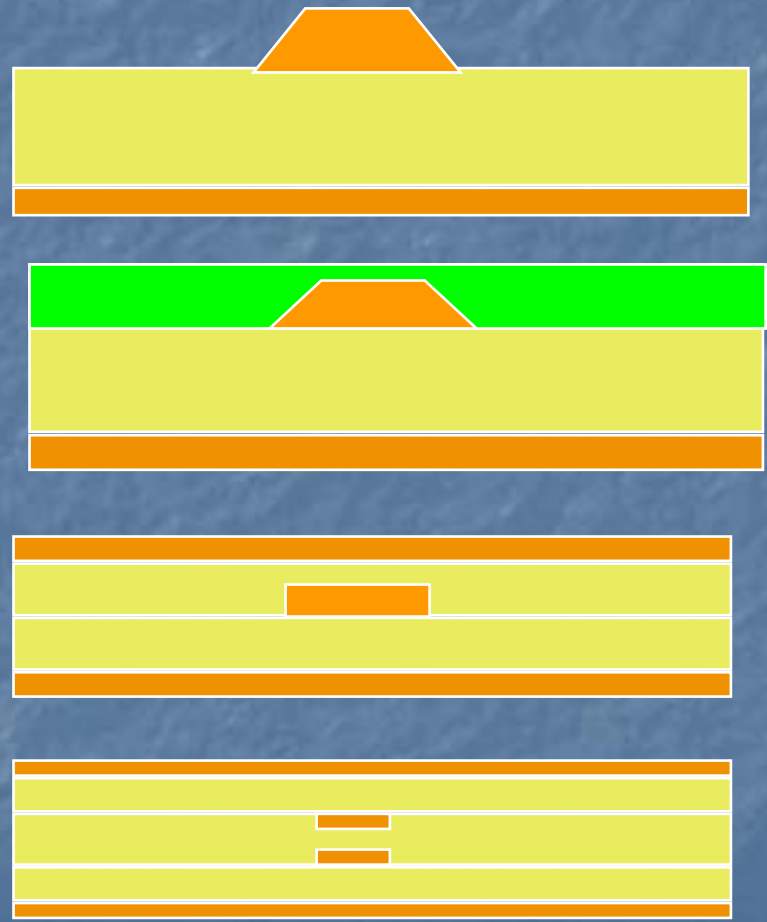
Types of constructions – single ended

Surface microstrip

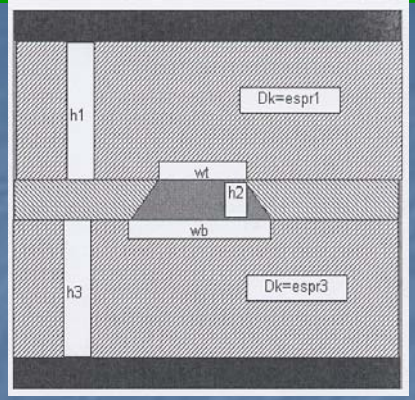
Coated microstrip

Stripline

Dual stripline



Strip-line Model



rickn - Streamline 1.6

title: single_ended_stripline
h1 is the dielectric thickness top reference plane to trace
h2 is the copper thickness of the trace
h3 is the dielectric thickness of the trace to the bottom reference plane
wt is the trace width at the top
wb is the trace width at the bottom
epsr1 is the dielectric constant between top reference plane and trace
epsr3 is the dielectric constant between bottom reference plane and trace

CUST:	P/N:			
type=gen	units=mil	freq=0.500e+09		
layers=3				
epsr1=4.0	tand1=1.400e-02	**h1=5.0**		
epsr2=3.000e+00	tand2=2.000e-02	**h2=1.28**		
epsr3=4.0	tand3=1.400e-02	**h3=7.56**		
ncond=1				
ntraces1=1				
layer=2	**wt=5.0**	**wb=5.5**	xcord=0.000e+00	sigma=5.800e+07
sigmagndtop=5.800e+07	gndthicknesstop=1.3			
sigmagndbottom=5.800e+07	gndthicknessbottom=1.3			
skin=y				

Impedance: 47.95 Skin Effect: 5.502e-004 Total Impedance: 49.6006

Total Impedance: 49.6006

Does soldermask affect Impedane?

"YES IT DOES"

Remember that soldermask, in almost all cases, will exist over the impedance traces on microstrip designs. If a dry-film mask is used this could be anywhere from 3-4 mils thick and could lower the impedance value as much as 7 ohms. Typical thickness of an LPI mask over the traces is .5 mil and the impedance value is only affected typically by 2 ohms. Due to very fine lines/spaces these days, dry-film soldermask is rarely used any longer.

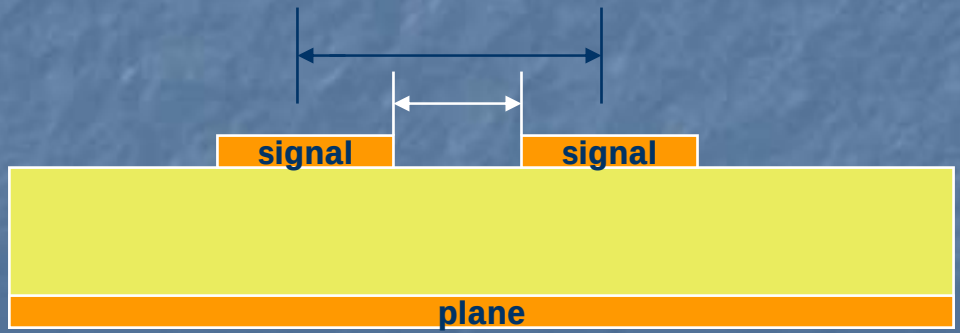
ANSWER!

- ABSOLUTELY NOTHING!!!!!! (Depending on who you talk to!!!!)

Most vendors would need to use a thickness of 4.2 to 4.5 nominal value to support this requirement. This would not have that much of an affect except in the case of micro-strip and dual-strip-line configurations. For micro-strip a line width of approximately 7 mils would be needed and for dual-strip-lines 5 mils to support this dielectric thickness. It also will affect the overall thickness of the board. There are many boards out there that do not meet this requirement for one reason or another and they work perfectly fine.

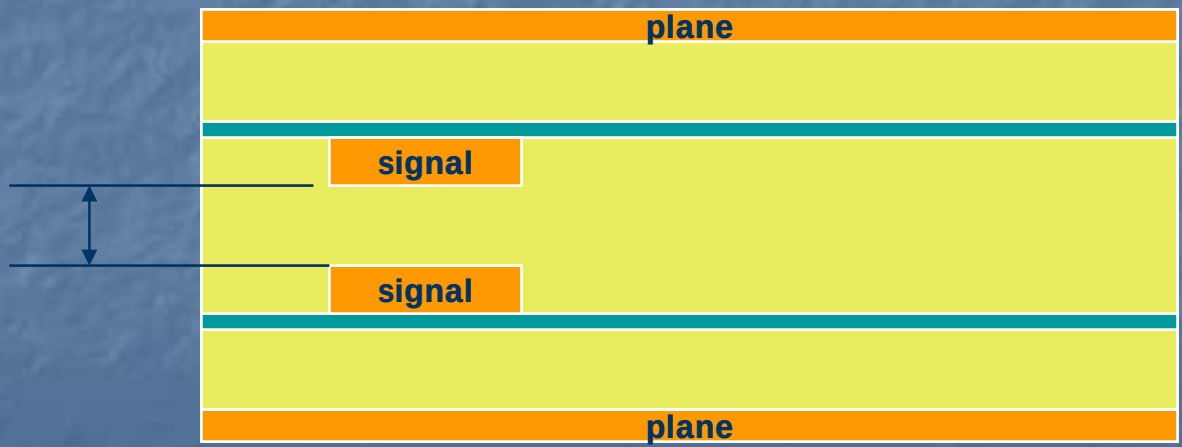
Differential Configuration: Edge-Coupled

The added importance of this configuration is the edge-edge spacing or center-center (pitch) of the two traces. If the traces are too far apart they will not couple to one another for EMI or noise considerations. A good rule of thumb is no more than 4x the trace width.

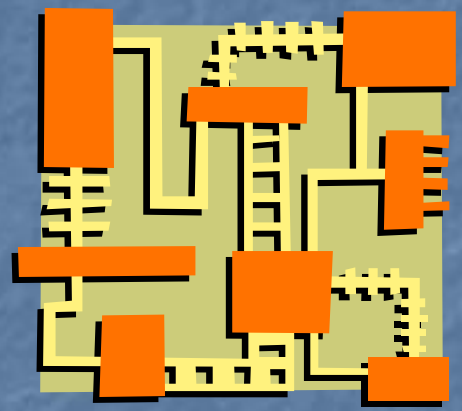


Broadside Configuration

- The added important factor of this configuration is the dielectric separation between the traces.

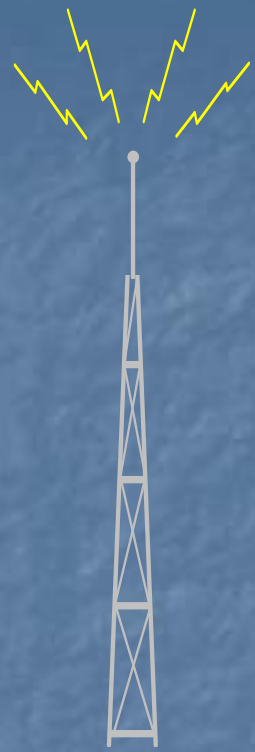


•Impedance Quality Factors



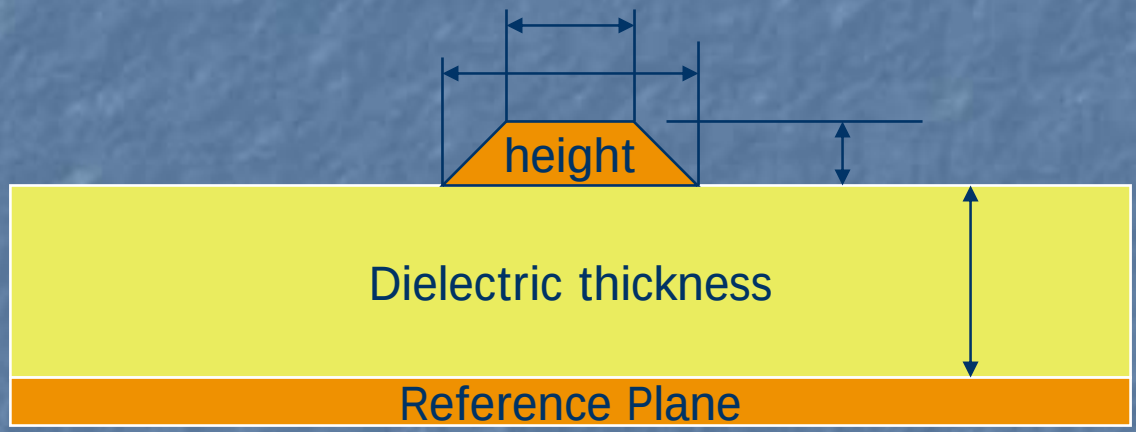
- Model reliability
- Coupon Integrity
- Measurement Integrity
- Process control and capability
- Defined work instructions
  - Training
  - Certification
- Lab analysis – cross section accuracy
- Measurement based modeling – “correlate model to physical structures”
- Feedback loop to planning or process using statistical analysis
- Engineering Impdedance seminars from designer viewpoint
- Future technology – impact of HDI or optoelectronics??

Most Critical Impedance Factors!



- Width of circuit trace
- Thickness of circuit trace
- Dielectric thickness
  - thickness of core, prepreg or solder mask around the circuit trace.

Impedance Factors



Additional factors to consider!

1. Dielectric Constant (Dk) of the material being used.

   This is sometimes known as Er. It is the ability of a material to hold an electromagnetic charge with air or space as 1. This is a function of the materials (resin, glass, soldermask, and air) that a circuit passes a signal through. Typical Dk's for circuit boards built with FR4 material range from 4.2 to 4.8.

2. Skin (AC flow is mostly near the outer surface of a solid electrical conductor.

3. Soldermask thickness and it's Dk value.

4. Trapezoid configuration of the traces.

Importance of dielectric thickness and line width

- Dielectric thickness is a function of core/prepreg selection and lamination parameters.
- Line width is a result of plotting, imaging, developing, and etching.
- Dielectric thickness and line width are the two most important factors in meeting impedance values.

Etch Compensation/Etch Loss

- Line widths on the customer's data are increased on the fabricator's data to compensate for etch loss. The amount of increase is dependent on the copper weight of the layers. Due to this, etched features spacing is very important.

.004 line width

.005 line width

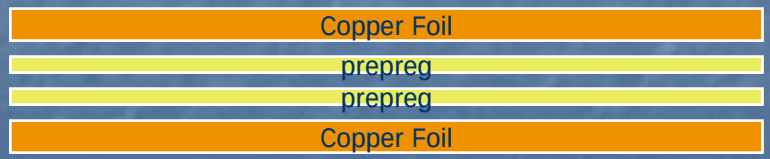
What is prepreg (b-stage)?

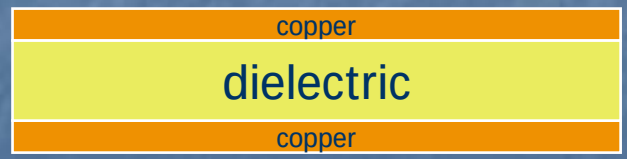
- Prepreg is a glass cloth that contains a percentage of resin that comes in various thicknesses. Some of the most notable thicknesses are:

*106 = .0023”
*1080 = .0031”
*2113 = .0041”
*2116 = .0045”
*7628 = .0074”

What is core material (C-Stage)?

Core material is a makeup of various styles of prepreg to a designated thickness. The prepreg is laminated with a designated type of copper foil and weight, using heat and pressure and then cured. For example: Thin cores are normally made up with a single-ply of prepreg. A .003 core would use a single ply of 2113 and .004 core, a single ply of 2116. Thicker cores are made up of multiple plies of prepreg such as .006 core. This would take a single ply of 1080 and a single ply of 2113.





Controlling Dielectric Thickness

- Controlling the thickness in critical impedance areas is dependent on the layer configuration; the copper percentage of that layer, and the copper height (thickness). This is known as loss to fill. This more-so involves the prepreg areas rather than the core areas.

- For example:

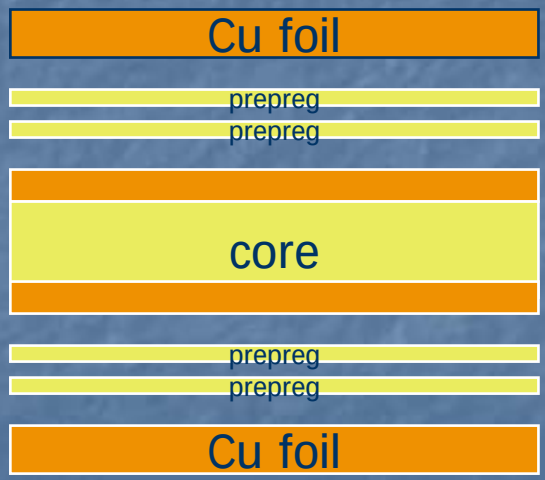
- Signal layer is typically 10% copper
- Mixed layer is typically 40-50% copper
- Plane layer is typically 80% copper.

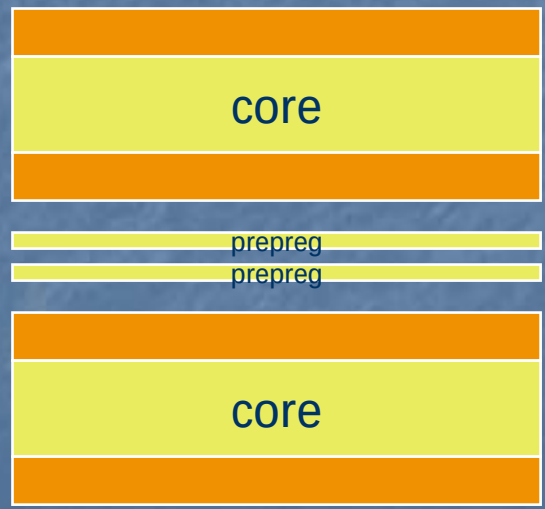
LOSS TO FILL RATIO

- Loss to fill is the thickness of the prepreg after the lamination process, when the resin has been squeezed from the layers and cured.

Cap (core) Construction vs Foil

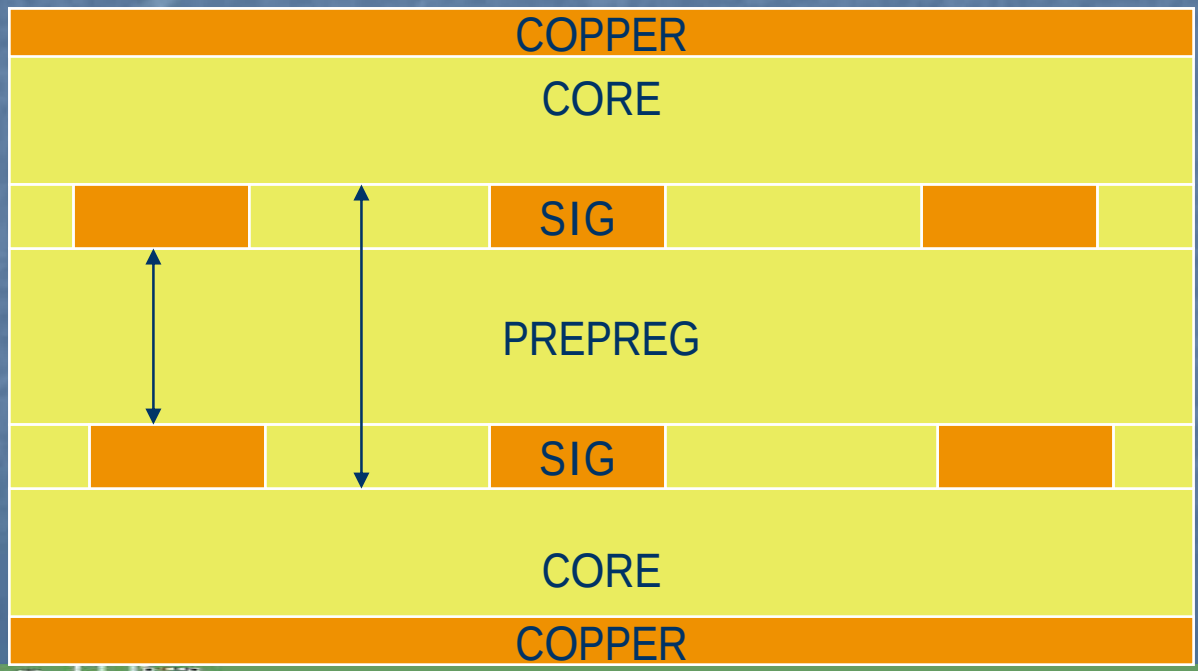
- Most board fabricators prefer to use a “foil” construction stackup instead of core.





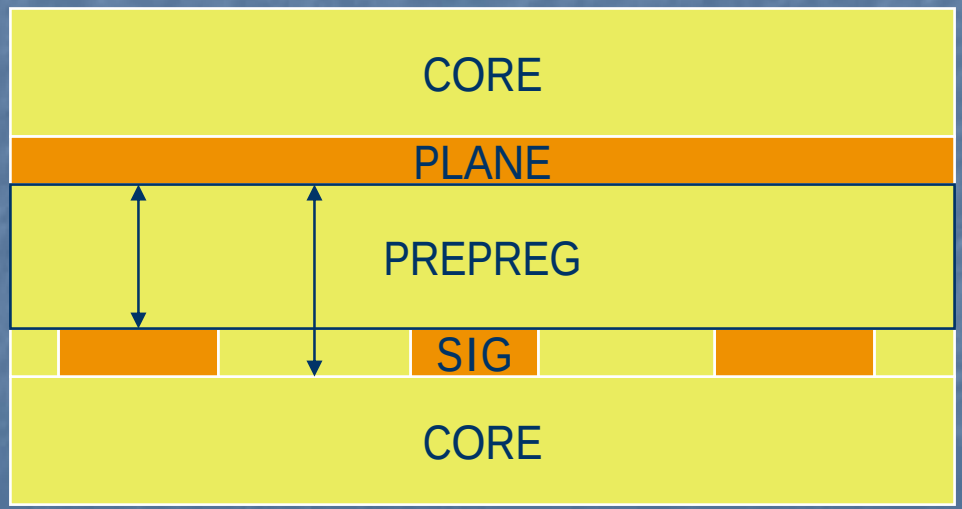
Signal against Signal

- Based on this configuration type you will see your greatest loss in dielectric:



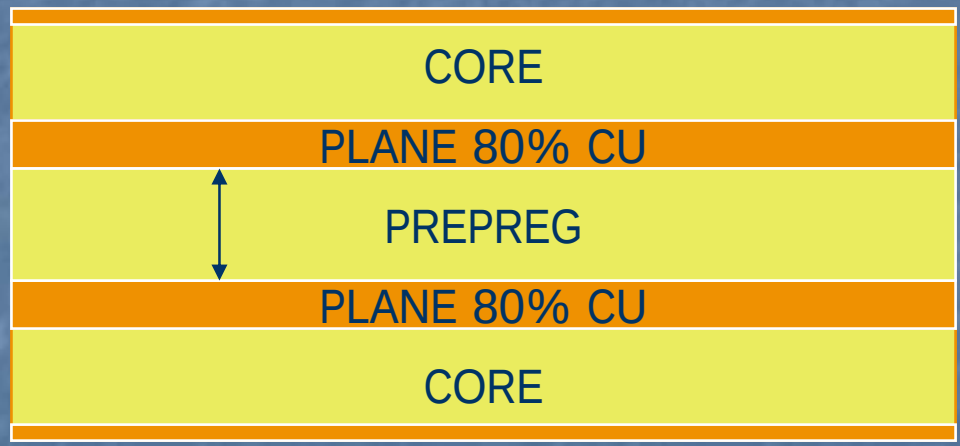
Plane against Signal

- With this type of configuration we see a little more loss in critical thickness:



Plane against Plane

- When you have this type of configuration (which is not critical for impedance) you will see minimal loss value.



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Thickness Model

Lyr #	Cu Wt	Thickness	% Cu	Fill Req	Core Thk	Preg Style	# Plys	Preg Thk	Glass Thk	Spacing	
1	0.5	0.00064	F	0		106-75%	0	0	0	0.002972	0.00
						1080-65%	1	0.0031	0.0025	OK	4.00
			Dk	4.00		2113-57%	0	0	0		0.00
						2116-56%	0	0	0		0.00
2	0.5	0.00064	0.8	0.000128		7628-50%	0	0	0		0.00
				4.37	0.005						
3	0.5	0.00064	0.2	0.000512		106-75%	0	0	0	0.00756	0.00
						1080-65%	0	0	0	OK	0.00
			Dk	3.80		2113-57%	2	0.0082	0.0058		3.80
						2116-56%	0	0	0		0.00
4	0.5	0.00064	0.8	0.000128		7628-50%	0	0	0		0.00
				4.37	0.005						
5	0.5	0.00064	0.8	0.000128		106-75%	0	0	0	0.00756	0.00
						1080-65%	0	0	0	OK	0.00
			Dk	3.80		2113-57%	2	0.0082	0.0058		3.80
						2116-56%	0	0	0		0.00
6	0.5	0.00064	0.2	0.000512		7628-50%	0	0	0		0.00
				4.37	0.005						
7	0.5	0.00064	0.8	0.000128		106-75%	0	0	0	0.002972	0.00
						1080-65%	1	0.0031	0.0025	OK	4.00
			Dk	4.00		2113-57%	0	0	0		0.00
						2116-56%	0	0	0		0.00
8	0.5	0.00064	F	0		7628-50%	0	0	0		0.00

CU THK = 0.00512 CORE = 0.015 PREG = 0.021064

OVERALL THICKNESS = 0.041184

Lyr #	Cu Wt	Thickness	% Cu	Fill Req	Core Thk	Preg Style	# Plys	Preg Thk	Glass Thk	Spacing	
1	0.5	0.00064	F	0		106-75%	0	0	0	0.002844	0.00
						1080-65%	1	0.0031	0.0025	OK	4.00
			Dk	4.00		2113-57%	0	0	0		0.00
						2116-56%	0	0	0		0.00
2	1	0.00128	0.8	0.000256		7628-50%	0	0	0		0.00
				4.37	0.005						
3	1	0.00128	0.2	0.001024		106-75%	0	0	0	0.00692	0.00
						1080-65%	0	0	0	OK	0.00
			Dk	3.80		2113-57%	2	0.0082	0.0058		3.80
						2116-56%	0	0	0		0.00
4	1	0.00128	0.8	0.000256		7628-50%	0	0	0		0.00
				4.37	0.005						
5	1	0.00128	0.8	0.000256		106-75%	0	0	0	0.00692	0.00
						1080-65%	0	0	0	OK	0.00
			Dk	3.80		2113-57%	2	0.0082	0.0058		3.80
						2116-56%	0	0	0		0.00
6	1	0.00128	0.2	0.001024		7628-50%	0	0	0		0.00
				4.37	0.005						
7	1	0.00128	0.8	0.000256		106-75%	0	0	0	0.002844	0.00
						1080-65%	1	0.0031	0.0025	OK	4.00
			Dk	4.00		2113-57%	0	0	0		0.00
						2116-56%	0	0	0		0.00
8	0.5	0.00064	F	0		7628-50%	0	0	0		0.00

CU THK = 0.00896 CORE = 0.015 PREG = 0.019528

OVERALL THICKNESS = 0.043488

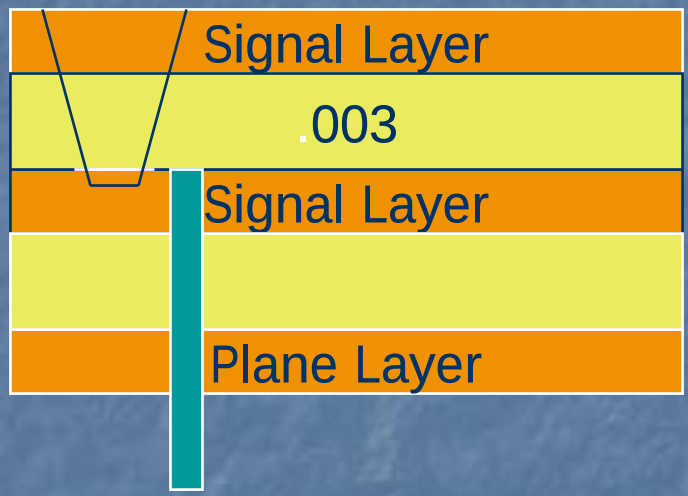
IPC-6012 MIN. DIELECTRIC

- Par 3.6.2.15: "The minimum dielectric spacing shall be specified in the procurement documentation (print). If the spacing and the number of reinforcing layers are not specified, the minimum dielectric spacing is 90um (.0036") and the number of reinforcing layers may be selected by the supplier. When the nominal dielectric thickness on the drawing is less than 90 um, the minimum dielectric spacing is 25 um (.001") and the number of reinforcing layers may be selected by the supplier.

- WHAT DOES THIS MEAN?

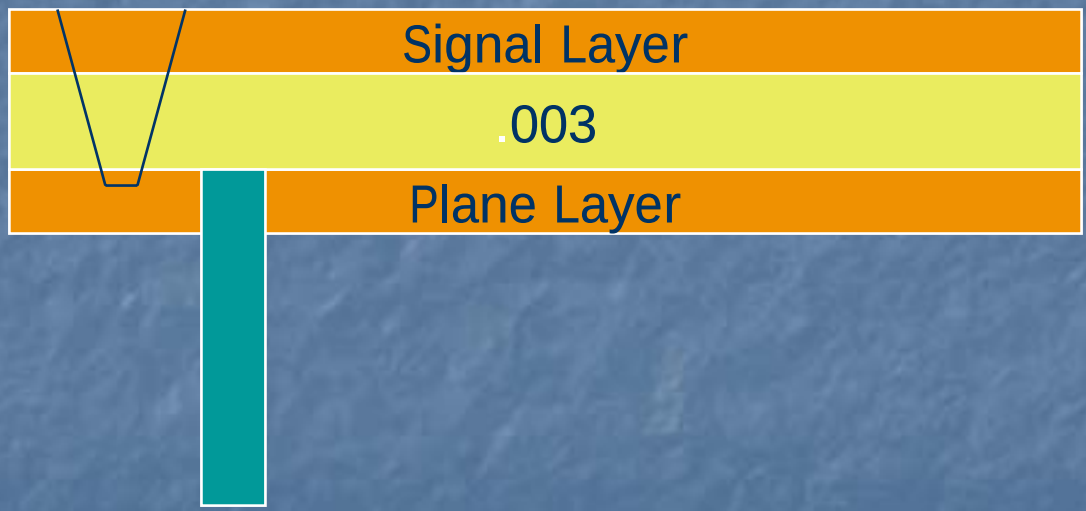
Micro-strip Imped with Micro-Vias/Buried Vias

- This configuration is not recommended:



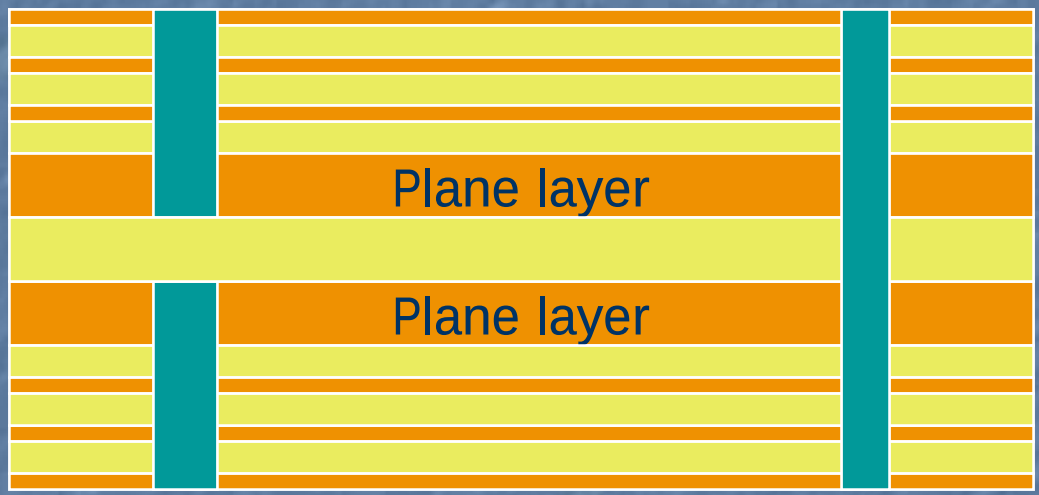
Micro-Strip Imped with Micro-vias/Buried Vias

- This is recommended:



Marrying Multiple Sub-Assemblies

- Same theory applies:



Hallmark Circuits, Inc.

Typical Stackup Document

HALLMARK CIRCUITS, INC.
Time-Critical Printed Circuit Board Specialists

Customer:	HALLMARK	**Part Number:**		**Rev:**		**Dk Value:**	4.0
Contact:		**Material Type:**	FR406 (Tg = 170 C)	**Lamination Thickness (nom):**	0.058	**Preparation By:**	*Rick Norfolk*
Telephone:		**Impedance Type:**		**Overall Thickness (nom):**	0.062	**Preparation Date:**	1/21/2006 10:17
# of Lyrs:	8	**Impedance Type:**		**HCI#:**		**Pass #:**	

Layer #	Type sig/pln	Base Cu Weight (oz)	Total Thickness	Dielectric Thickness (mils)	Dielectric Material (Cores/Prepreg)	S/E IMPED. Fin. L/W	S/E IMPED. Value	DIFFERENTIAL IMPED. Fin. L/W	DIFFERENTIAL IMPED. Pitch *	DIFFERENTIAL IMPED. Value	Ref Planes
1	SIG	0.5	0.0022		Base Cu + Plating	5	50	4	14	100	L2
				0.003	1x1080 prepreg						
2	PLN	0.5	0.00064								
				0.005	Core						
3	SIG	0.5	0.00064			5.5	50				L2, L4
				0.0076	2x2113 prepreg						
4	PLN	0.5	0.00064								
				0.005	Core						
5	PLN	0.5	0.00064								
				0.0076	2x2113 prepreg						
6	SIG	0.5	0.00064			5.5	50				L5, L7
				0.005	Core						
7	PLN	0.5	0.00064								
				0.003	1x1080 prepreg						
8	SIG	0.5	0.0022		Base Cu + Plating	5	50	4	14	100	L7

NOTES:
1. Prepreg thickness specified above are estimated loss to fill values.
2. Final thickness, unless otherwise specified, is to be measured over soldermask and plating.
3. Blind/Buried Vias: None

* Pitch: Center-Center of the traces.

NOTE: THIS STACKUP WILL NOT MEET THE MINIMUM .0035" DIELECTRIC REQUIRED BY IPC-6012. ACCEPTANCE OF THIS STACKUP IS CUSTOMER APPROVAL THAT THE DIELECTRIC THICKNESS MAY BE LESS THAN THE .0035" MINIMUM.

Mechanical Print Note

- * Layers 4,5,8, and 9 using 5 mil line width designed to achieve 50 ohm single-ended impedance. Layers 1 and 8 using a 5 mil line width designed to achieve 50 ohm single-ended impedance and 4 mil line with .012 edge-edge spacing (or .016 pitch) to achieve 100 ohm edge-coupled differential impedance. Vendor may modify lines/dielectrics as needed to fit their processes to achieve required impedance values and overall board thickness.

What is Time Domain Reflectometry?

- TDR is the analysis of a conductor by sending a pulsed signal into the conductor and then examining the reflection of that pulse.

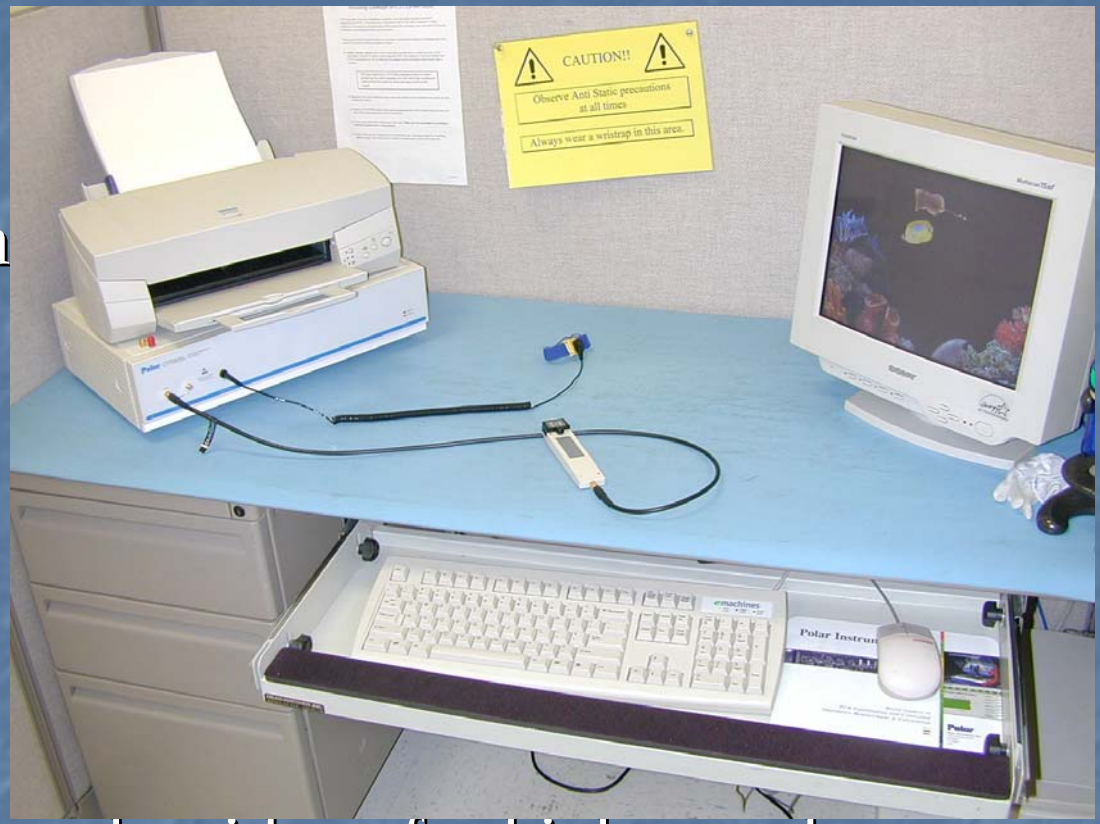
SAMPLE TDR COUPON

- TDR measurements are typically done on coupons and not on the individual boards.
- Coupons are strategically placed onto a production panel and is representative of the board design.

Hallmark Circuits, Inc.

Polar CITS-500s

- TDR Test System
  Single-ended
  Differential
  RAMBUS©



- Confirms modeling algorithms for high-speed designs
- Integral in the development of new designs

Recommendations

- If you are declaring that the board is a “designed” impedance, you should specify the finished critical line widths and the dielectric thickness that the fabricator is to maintain. Please keep in mind that the fabricator will not normally do any TDR testing on the board and will maintain your parameters only. The impedance value obtained is the OEM’s responsibility.

- Do not handcuff the fabricator. Tell them what impedance value you are targeting with what line widths and leave the rest to them. On your prints, please specify the pitch or edge-edge spacing for diff pairs. Allow them to modify the dielectrics/lines as needed for their processes to achieve the required impedance by placing a note on the fabrication drawing allowing this. Remember, they are the ones responsible for meeting the required impedance.

- Work with your vendor as much as possible during the design stage to establish a viable stackup. Partnership with your vendor during the initial design phase is very important. It’s truly a bummer to find out after all your hard work that the impedance you are looking for cannot be met with your design criteria.

•Information sources

- Engineering Solutions, “Controlled Impedance Workshop”,Bill Fujitsubo
- IPC “High Speed Design (IPC - D - 317)”
- “High Speed Design Workbook”, Lee Ritchey
- IPC “High Speed, High Frequency Workshop”